

UNIT-1 Basic of OP-AMP

BJT

(IC, Transistor)

IC:

[Inductor does not fabricated inside the IC because of size]

IC is a Integrated circuits it consists of active and passive components integrated in a single chip.
(Res, cap)
Ind

Advantages:

- (i) Minature in size
- (ii) compactability
- (iii) More reliable (since we ^{not} have soldering)
- (iv) ↑ Speed
- (v) Reduced power consumption

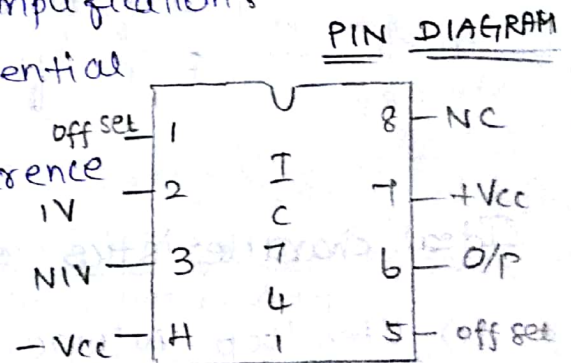
OP-AMP:

operational amplifier it manipulates all mathematical operation with amplification.

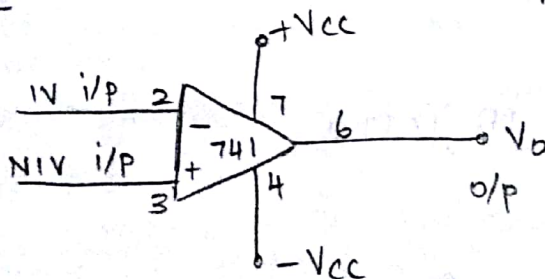
It is a high gain differential

We need two power supply

amplifier which amplifies difference b/w two inputs.



SYMBOL:



To reduce leakage current the 1 & 5 pin is used.

[In inside itself it compensate and give clear o/p] - used in lab.

Packages:

- (1) Flat package (eg: memory card) ^{more reliable}
- (2) Dual Inline package (eg: digital IC) ^{easy to mount}
- (3) Metal can package (like transistor)

IC identification:

XX TH Y Z

manufacture name type of IC Package type temp range

Where H is used

For 1st 2 alphabets

MA → Fairchild
 LM, LH, LF → National Semiconductor
 MC, MFC → Motorola
 SN → Texas instrument
 BB → Burr Brown

In the place of 'Y'

C → commercial purpose (0°-70°)
 I → Industrial (-25° to 85°)
 M → military (-55°-+125°)

operating range

In the place of 'Z'

D → Dual Inline package
 F → flat package

Ideal characteristics of OP-AMP: (2m)

→ do not having feedback (o/p to i/p signal)

(1) Open loop voltage gain is infinite

$$10^5 = 100k$$

$$A_{OL} = \infty$$

(2) Input impedance is infinite

op-amp → Res ↑

doesn't consume any power

$$R_i = \infty$$

→ deliver the power, in (MOSFET)

(3) Output impedance is 0

$$R_o = 0$$

(4) CMRR = ∞

$$A_D / A_{CM}$$

1MHz

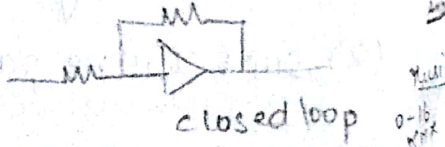
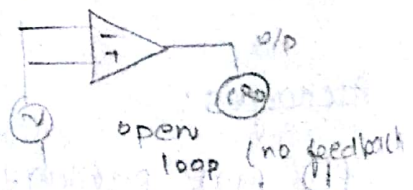
[able to reject the noise]

(5) Bandwidth is infinite

(6) Slew rate is infinite

note:

we can give any signal ac or dc. in op-amp



speech - 0-8 KHz
frequency → speed

Transistor,
(1) maximum o/p is depends on the power supply.

eg: Power supply 15

15/12/17 $V_p = 10V$ gain = $2V = 20V$

o/p is
o/p $\Rightarrow$ saturates at 15
itself

(1) Open loop:

$A_{of} = \infty$ which means that the gain of OP-AMP is very much high hence the o/p is saturated to any one of the voltage.

$$+V_{sat} \approx +V_{cc} \quad -V_{sat} \approx -V_{cc}$$

Invert mode = o/p is square wave irrespective of input.

(2) $R_i = \infty$, it consumes no current,

i.e) All the signal power is deliver to the next stage.

(3) $R_o = 0$, the entire signal is deliver to the loading stage.

(4) $CMRR = \infty$, $\frac{A_D}{A_C}$ the OP-AMP has only differential A_D , the common mode gain is almost 0, $A_C \approx 0$ which makes very high CMRR.

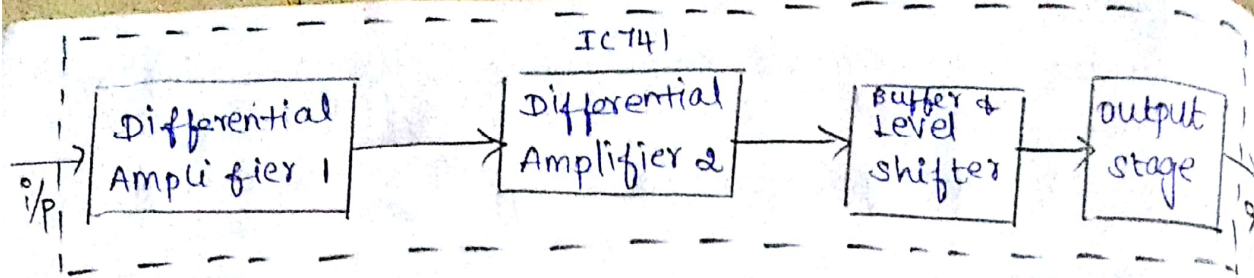
(5) operating range is very high in OP-AMP,

i.e) It can access signal from 0- ∞ Hz without any attenuation.

(6) slew rate:
change in voltage with respect to time is known as slew rate. $\left[\frac{dv}{dt} \right]$ [no delay]

General operational amplifier stages:

Internal block diagram:



16/12/17

Differential amplifier:

(1) Op-AMP consists of differential amplifier which has high gain at differential mode and cancelled the common mode signal which suppress the undesired noise on the op-amp.

(2) Another Aim is this amplifier provides high i/p impedance and it has no coupling capacitor.

(3) A differential amplifier has 4 configuration

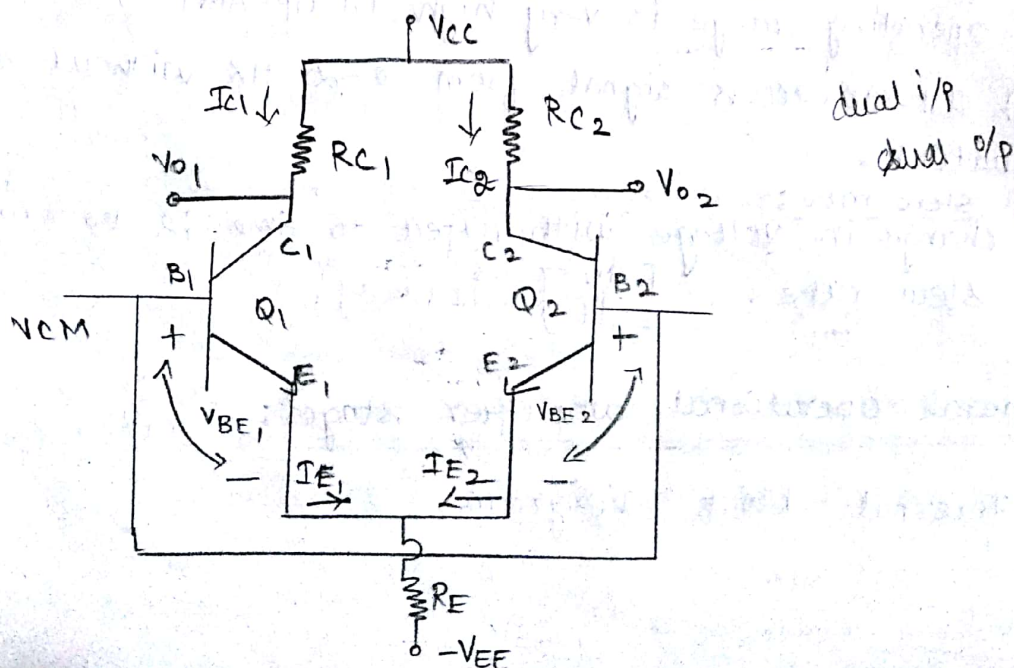
- (i) Dual input, dual o/p
- (ii) Dual input, single o/p $\rightarrow$ in op/amp
- (iii) Single input, Dual o/p
- (iv) Single input, single o/p

Note:

Differential amplifier 1 $\Rightarrow$ Dual input, Dual o/p balanced.

Differential amplifier 2 $\Rightarrow$ Dual input, single o/p

Case (1): common mode differential amplifier



Base 1 and Base 2 are joined together and given an voltage V_{C1} . Since the Transistor are identical & symmetric the current divides equally.

$$i.e) I_{E1} = I_{E2} = \frac{I_Q}{2} \quad \text{--- (1)}$$

The current through the collector is given by

$$I_{C1} = \alpha I_{E1} \quad \text{--- (2)} \Rightarrow \frac{\alpha I_Q}{2}$$

$$I_{C2} = \alpha I_{E2} \quad \text{--- (3)} \Rightarrow \frac{\alpha I_Q}{2}$$

by applying KVL, @ Q1

$$V_{CC} = I_{C1} R_{C1} + V_{O1} \quad \text{--- (4)}$$

Sub I_{C1} in (4)

$$V_{CC} - \frac{\alpha I_Q R_{C1}}{2} = V_{O1} \quad \text{--- (5)}$$

apply KVL, @ Q2

$$V_{CC} = I_{C2} R_{C2} + V_{O2}$$

$$V_{O2} = V_{CC} - I_{C2} R_{C2} \quad \text{--- (6)}$$

$$V_{O2} = V_{CC} - \frac{\alpha I_Q R_{C2}}{2}$$

The o/p of differential amplifier is the difference in voltage,

$$V_o = V_{O1} - V_{O2}$$

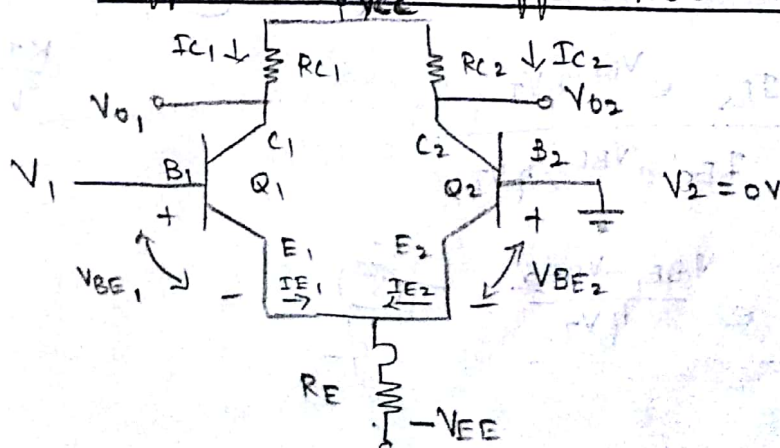
Since ckt is symmetric $R_{C1} = R_{C2} = R_C$

$$V_o = V_{CC} - \frac{\alpha I_Q R_C}{2} - V_{CC} + \frac{\alpha I_Q R_C}{2}$$

$$V_o = 0$$

Hence differential amp. provide no common mode gain.

Case(2) : Difference mode differential amplifier: (i/p, 2 o/p)



operation:

$Q_1 + Q_2$ 180° phase shifted.

Initially Q_2 is off since $V_Q = 0$. The entire current (I_Q) flows through Q_1 .
i.e) Q_1 is ON.

Assume $V_1 = 1V$ V_{BE1} is 0.7 consumed by the transistor. Hence 0.3V is obtained at the o/p.
And so Q_2 is OFF.

If -ve voltage is applied to be '1'. Q_2 is ON and Q_1 is OFF. so the entire current flows through Q_2 .

19/12/17

The general diode equation is for the transistor

$$I = I_0 e^{\frac{V}{\eta V_T}} \quad \begin{array}{l} \eta = 1, 2 \rightarrow \text{germanium} \\ \downarrow \\ \text{silicon} \end{array} \quad \begin{array}{l} V_T = \text{thermal} \\ \text{voltage} \end{array}$$

consider the emitter current,

$$I_E = I_{ES} e^{\frac{V_{BE}}{\eta V_T}} \quad \text{--- (1)}$$

Relation b/w collector current + emitter current,

$$I_C = \alpha I_E \quad \text{--- (2)}$$

consider transistors Q_1, Q_2 i.e) I_{C1}

$$I_{C1} = \alpha_F I_{E1}$$

$$I_{C1} = \alpha_F I_{ES} e^{V_{BE1}/\eta V_T} \quad \text{--- (3)}$$

likewise,

$$I_{C2} = \alpha_F I_{ES} e^{V_{BE2}/\eta V_T} \quad \text{--- (4)}$$

$$V_T = \frac{11600}{T} \frac{KT}{q}$$

$$\frac{I_{C1}}{I_{C2}} = \frac{\alpha_F I_{ES} e^{V_{BE1}/\eta V_T}}{\alpha_F I_{ES} e^{V_{BE2}/\eta V_T}}$$

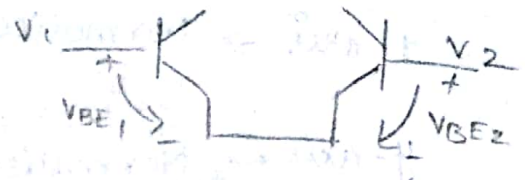
$$\frac{I_{C1}}{I_{C2}} = e^{\frac{V_{BE1} - V_{BE2}}{\eta V_T}} \quad \text{--- (5)}$$

consider the circuit

Apply KVL,

$$V_1 - V_{BE1} + V_{BE2} - V_2 = 0$$

$$V_1 - V_2 = V_{BE1} - V_{BE2} \quad \text{--- (6)}$$



$$I_Q = I_{E1} + I_{E2}$$

$$= \frac{I_{C1}}{\alpha_F} + \frac{I_{C2}}{\alpha_F}$$

$$= \frac{I_{C2}}{\alpha_F} \left[1 + \frac{I_{C1}}{I_{C2}} \right] \quad \text{--- (7)}$$

$$I_C = \alpha_F I_E$$

$$I_E = I_C / \alpha_F$$

I_{C1}

sub (6) in (7)

$$I_Q = \frac{I_{C2}}{\alpha_F} \left[1 + e^{\frac{V_{BE1} - V_{BE2}}{\eta V_T}} \right] \quad \text{--- (8)}$$

$$I_{C2} = \frac{\alpha_F I_Q}{1 + e^{\frac{V_{BE1} - V_{BE2}}{\eta V_T}}}$$

in short $\frac{V_{BE1} - V_{BE2}}{\eta V_T}$

taking $\frac{I_{C1}}{\alpha_F}$ from (7)

$$V_d = V_{BE1} - V_{BE2}$$

$$\frac{I_{C1}}{\alpha_F} \left[1 + \frac{I_{C2}}{I_{C1}} \right]$$

$$I_{C2} = \frac{\alpha_F I_Q}{1 + e^{V_d / \eta V_T}}$$

$$= \frac{I_{C1}}{\alpha_F} \left[1 + \frac{1}{e^{\frac{V_{BE1} - V_{BE2}}{\eta V_T}}} \right]$$

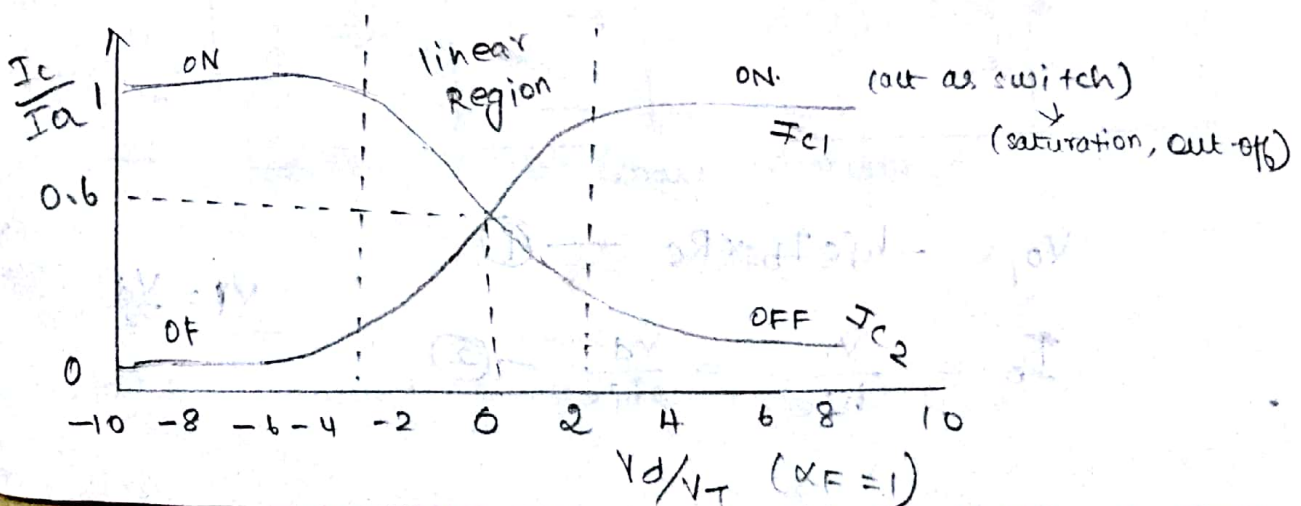
$$= \frac{I_{C1}}{\alpha_F} \left[1 + e^{-\frac{V_{BE1} - V_{BE2}}{\eta V_T}} \right]$$

$$I_{C1} = \frac{\alpha_F I_Q}{1 + e^{-V_d / \eta V_T}}$$

$$I_{C1} = \frac{\alpha_F I_Q}{1 + e^{-\frac{V_{BE1} - V_{BE2}}{\eta V_T}}}$$

$$1 + e^{-\frac{V_{BE1} - V_{BE2}}{\eta V_T}}$$

Transfer Characteristic curve:



x-axis $\rightarrow$ Normalised i/p differential V_d

$\leftarrow$ (divided by some ref V_T) $\frac{V_d}{V_T}$ ($\alpha_T = 1$)

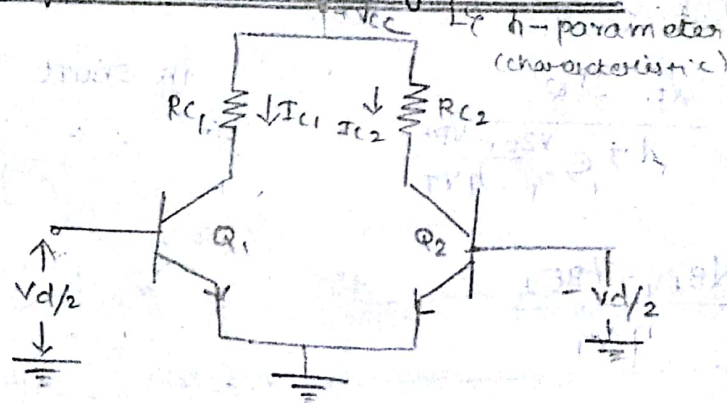
y-axis $\rightarrow$ Normalised collector at $\frac{I_C}{I_{CQ}}$
(to make uniformly we dividing reference V_T)

If V_d is greater than $+V_T$, $I_{C1} = \alpha I_Q$
 $I_{C2} \approx 0A$.

If V_d is less than $-V_T$, $I_{C1} \approx 0A$, $I_{C2} = \alpha I_Q$

blw $+V_T$ to $(-V_T)$ we get faithful amplification which is known as linear region. This also have automatic gain control which is done by varying I_Q .

20/12/17 Differential mode gain ADM: ACM:

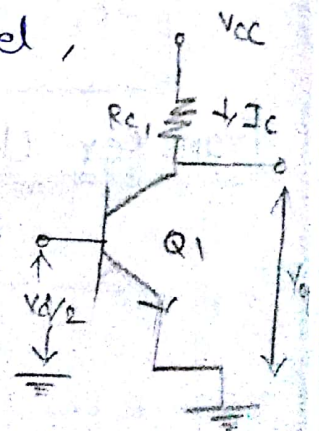
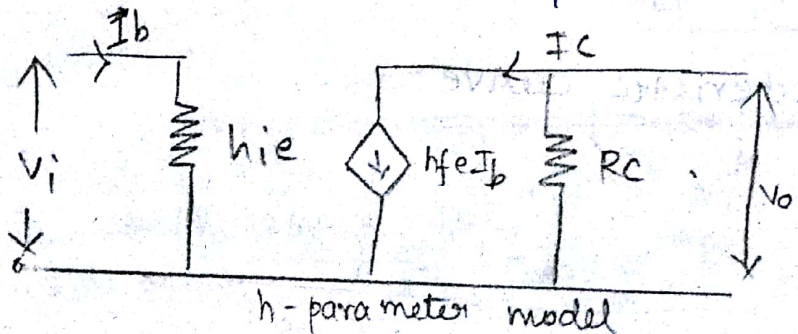


i/p 1 is given as $V_d/2$ (incremental voltage)

i/p 2 is given as $-V_d/2$ (decremental voltage)

used to analyse the difference mode gain,

Now consider the h-parameter model,



$$V_{O1} = -h_{fe} I_b \times R_C \quad \text{--- (1)}$$

$$I_b = \frac{V_i}{h_{ie}} = \frac{V_d}{2h_{ie}} \quad \text{--- (2)}$$

$$V_i = \frac{V_d}{2}$$

$$V_{o1} = -\frac{h_{fe} V_d R_c}{2 h_{ie}} \quad \text{--- (3)}$$

The Difference mode gain

$$A_{DM} = \frac{V_{o1} - V_{o2}}{V_d}$$

$$V_{o2} = \frac{h_{fe} V_d R_c}{2 h_{ie}} \quad \text{--- (4)}$$

(Aom above V_{o1} eq)

$$A_{DM} = \frac{-\frac{h_{fe} V_d R_c}{2 h_{ie}} - \frac{h_{fe} V_d R_c}{2 h_{ie}}}{V_d}$$

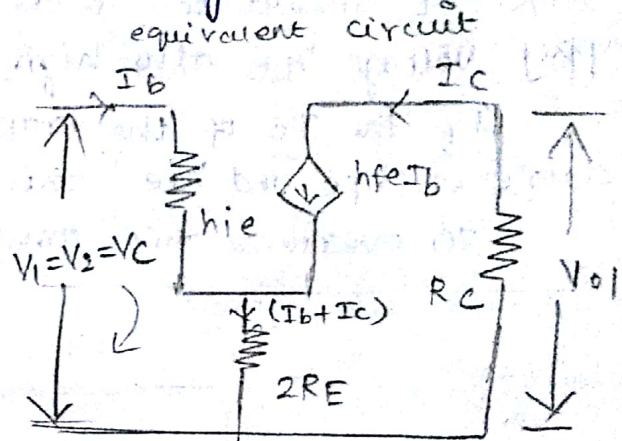
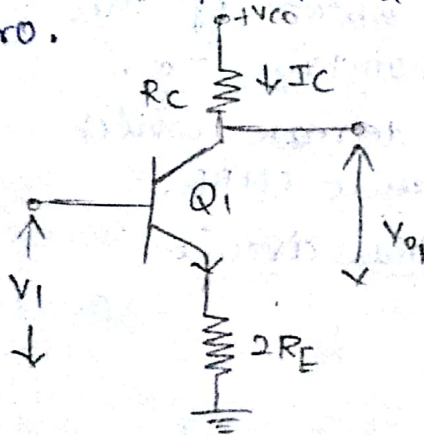
$$A_{DM} = -\frac{2 h_{fe} R_c}{2 h_{ie}}$$

for $\frac{V_d}{2}$ problem $\frac{V_d}{2}$

$$A_{DM} = -\frac{h_{fe} R_c}{h_{ie}}$$

Common mode gain A_{CM} : i/p = M

Both i/p's $V_1 + V_2$ are increasing and V_d is zero.



$$V_{o1} = -h_{fe} I_b \times R_c \quad \text{--- (1)}$$

$$V_c = I_b h_{ie} + [I_b + h_{fe} I_b] 2 R_E$$

$$= I_b [h_{ie} + (1 + h_{fe}) 2 R_E]$$

$$A_{CM} = \frac{V_{o1}}{V_c} = \frac{-h_{fe} I_b R_c}{I_b [h_{ie} + (1 + h_{fe}) 2 R_E]}$$

$$A_{CM} = \frac{-h_{fe} R_c}{[h_{ie} + (1 + h_{fe}) 2 R_E]}$$

R_E should be infinite
 $R_E = \infty$

CMRR - common mode Rejection Ratio

$$CMRR = \frac{A_{DM}}{A_{CM}} \quad \text{to get High CMRR}$$

A_{CM} should be Zero

common mode signal should be neglected

Note:

(1) To obtain High CMRR R_E should be very high
i.e) $A_{CM} = 0$

(2) The o/p voltage $V_{O1} = A_{DM} V_{DM} + A_{CM} V_{CM}$

$$V_{O2} = -A_{DM} V_{DM} + A_{CM} V_{CM}$$

21/12/17

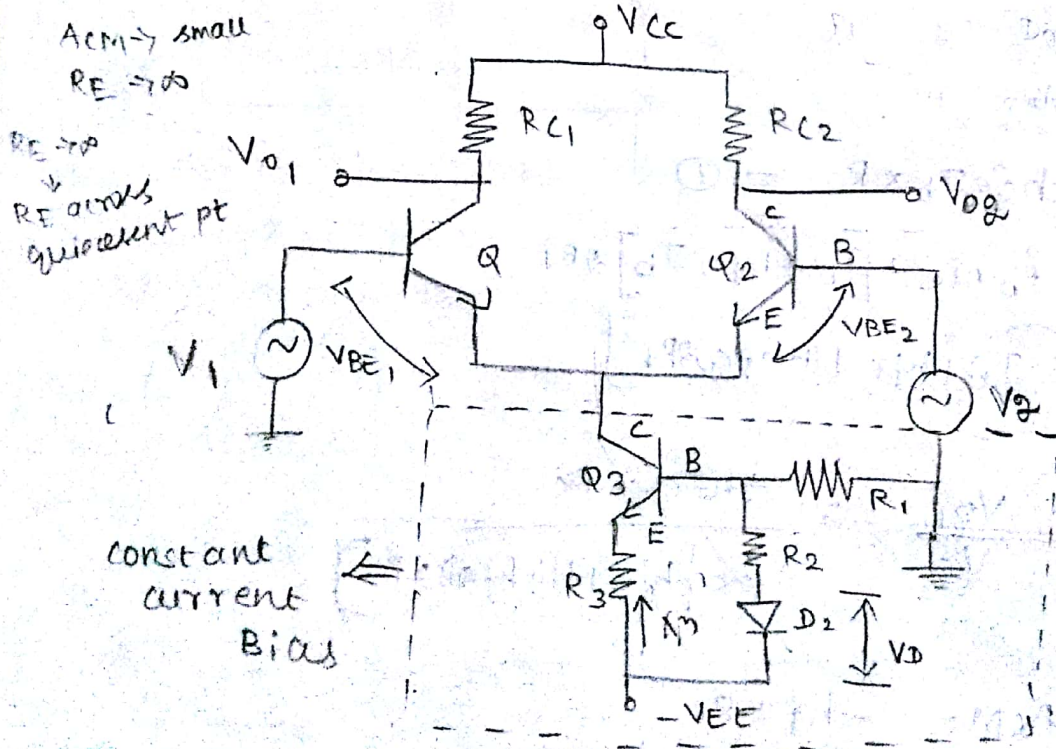
CIRCUITS TO IMPROVE CMRR: (Current mirror)

In conventional differential amp. to obtain high CMRR R_E should be made large, bcoz of this supply voltage V_{EE} also high to maintain I_Q .

If the I_Q of the transistor decrease which decrease h_{fe} and h_{ie} this will effect CMRR.

To overcome this constant bias circuit.

Constant bias circuit:

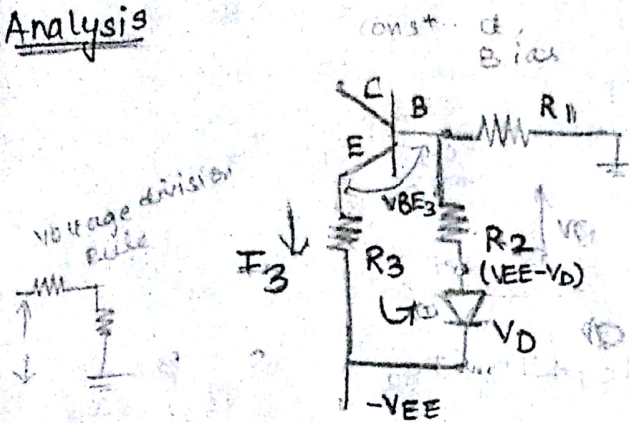


* The Resistance (R_E) is replaced by constant current Bias.

* The Diode is used to maintain the thermal stability.

* R_1, R_2, R_3 adjusted to provide constant current. even with small value of R_3

Analysis



$$V_{R2} = (V_{EE} - V_D) \frac{R_2}{R_1 + R_2} \quad \text{--- (1)}$$

Apply KVL,

$$V_{BE3} + I_3 R_3 = V_D + V_{R2}$$

$$V_{BE3} + I_3 R_3 = V_D + \frac{(V_{EE} - V_D) R_2}{R_1 + R_2} \quad \text{--- (2)}$$

$$I_3 R_3 = V_D + \frac{(V_{EE} - V_D) R_2}{R_1 + R_2} - V_{BE3}$$

$$I_3 R_3 = \frac{V_{EE} R_2}{R_1 + R_2} + V_D - \frac{V_D R_2}{R_1 + R_2} - V_{BE3}$$

$$I_3 R_3 = \frac{V_{EE} R_2}{R_1 + R_2} + \frac{V_D R_1}{R_1 + R_2} - V_{BE3} \quad \text{--- (3)}$$

R_1, R_2 can be adjusted so that $\frac{V_D R_1}{R_1 + R_2} \approx V_{BE3}$

$$\text{Hence } I_3 R_3 = \frac{V_{EE} R_2}{R_1 + R_2}$$

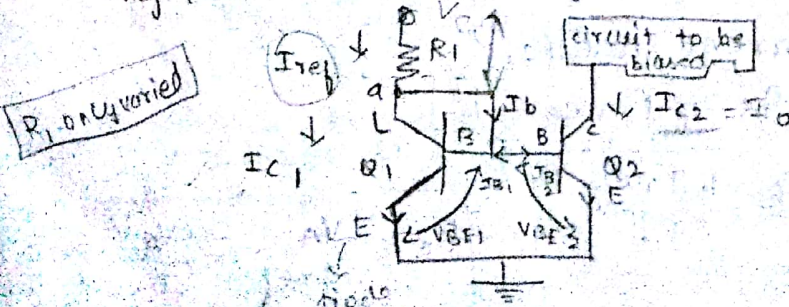
$$\text{current from the transistor } I_3 = \frac{R_2}{R_3 (R_1 + R_2)} \cdot V_{EE} \quad \text{--- (4)}$$

I_Q is a constant is independent of applied voltage $V_1 + V_0$. Hence the circuit improves CMRR, by dividing I_Q equally.

CURRENT MIRROR CIRCUIT (or) constant current source)

This circuit provides high impedance under AC condition. And provide high value of CMRR.

Only transistor $\rightarrow$ active region act as amplifier



$Q_1, Q_2 \rightarrow$ both are symmetrical
 $V_{BE1} = V_{BE2}$

22/12/17

Analysis:

Assume $V_{B1} = V_{B2}$, $I_{E1} = I_{E2} = I_{ref}$, $\beta_1 = \beta_2 = \beta$

$$I_{C2} = I_0$$

$$\frac{I_{C2}}{I_{C1}} = e^{\frac{V_{BE2} - V_{BE1}}{V_T}}$$

(from previous)

$$= e^0 = 1$$

$$I_{C2} = I_{C1} = I_0$$

Apply KCL at node a;

$$I_{ref} = I_{C1} + I_B \Rightarrow I_{C1} + I_{B1} + I_{B2}$$

collector current independent of

collector voltage in active region = $I_{C1} + 2I_{B1}$

$$= I_{C1} + 2 \frac{I_{C1}}{\beta}$$

$$= I_{C1} \left[1 + \frac{2}{\beta} \right]$$

$$I_{ref} = I_{C1} \left(\frac{2+\beta}{\beta} \right) \text{ --- (1)}$$

$$I_{ref} = I_0 \left(\frac{2+\beta}{\beta} \right)$$

$$I_{C1} = I_0$$

$$I_0 = I_{ref} \left(\frac{\beta}{2+\beta} \right)$$

$I_0 \approx I_{ref}$ (b/c β has large value in the fabrication)

Note: $\beta \gg 1$

$\frac{\beta}{2+\beta} \approx \text{unity}$ so only, $I_0 \approx I_{ref}$

$$I_{ref} = \frac{V_{CC} - V_A}{R_1}$$

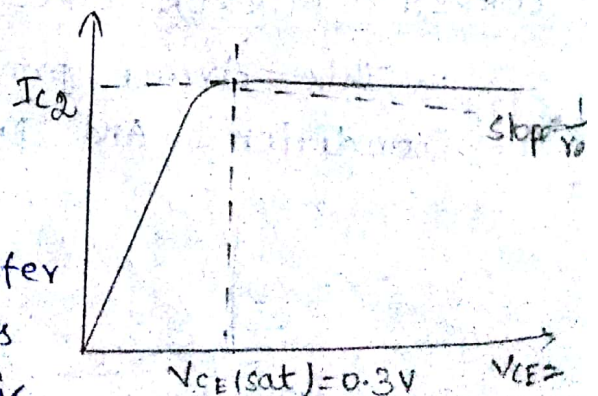
$V_A = V_{BE}$ (since the transistor Q_1 forms a diode)

$$I_{ref} = \frac{V_{CC} - V_A}{R_1}$$

$$I_{ref} = \frac{V_{CC} - V_{BE1}}{R_1}$$

↓

To obtain a proper current transfer ratio the area of Q_2 is 4 times that of Q_1 . so that $I_0 = 4I_{ref}$ is possible



$$R_0 = \frac{V_A}{I_{ref}} \approx \frac{V_A}{I_0}$$

from the graph,
when $V_{CC} > 0.3 V$, Q_2 is active and I_{C2} is constant

$V_A \rightarrow$ Early voltage (or) early effect voltage (channel width modulation)
depletion region towards Base [CB] $\downarrow$ Base emitter [TE modulation] $\downarrow$ LBBET

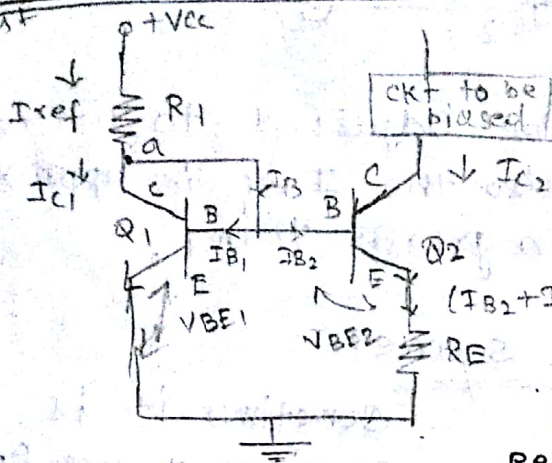
n p n

Transistor

doping (less concentration) towards Base

Base emitter [TE modulation] $\downarrow$ LBBET

Widlar current Source:



(1) The Basic current mirror has a limitation, that for low I_O the R_1 should be very high. $\downarrow I_B \downarrow R_1 \uparrow$

(2) Which cannot be fabricated economically.

(3) Hence Widlar current source with extra Emitter resistance (R_E) is used for low value currents.

Due to R_E , $V_{B2} < V_{B1}$; $I_{C2} < I_{C1}$, $I_O < I_{ref}$

$$\frac{I_{C2}}{I_{C1}} = e^{\frac{(V_{BE2} - V_{BE1})}{\eta V_T}}$$

taking $\ln$ on both sides (to neglect the $e^{\text{power term}}$)

$$\frac{V_{BE2} - V_{BE1}}{\eta V_T} = 2.303 \log \left(\frac{I_{C2}}{I_{C1}} \right)$$

$$\frac{I_{C1}}{I_{C2}} = e^{\frac{(V_{BE1} - V_{BE2})}{\eta V_T}}$$

$$\ln \frac{I_{C1}}{I_{C2}} = \frac{V_{BE1} - V_{BE2}}{\eta V_T}$$

$$V_{BE1} - V_{BE2} = V_T \ln \frac{I_{C1}}{I_{C2}} \quad \text{--- (1)}$$

Apply KVL for Emitter Base loop

$$V_{BE1} - V_{BE2} - (I_B + I_{C2}) R_E = 0$$

$$V_{BE1} - V_{BE2} = (I_B + I_{C2}) R_E \quad \text{--- (2)}$$

$$(I_{B2} + I_{C2}) R_E = V_T \ln \frac{I_{C1}}{I_{C2}}$$

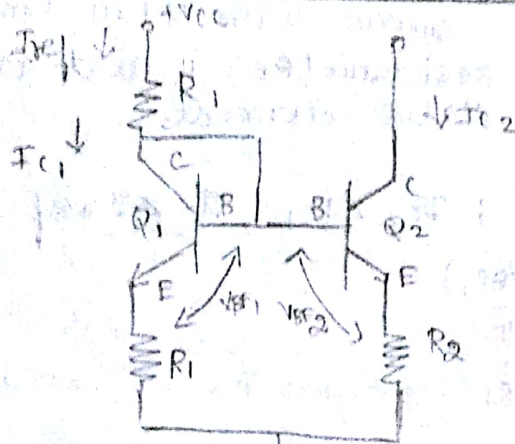
$$I_E = \frac{I_{C2}}{\beta} \left(\frac{I_{C2}}{\beta} + I_{C2} \right) R_E = V_T \ln \frac{I_{C1}}{I_{C2}}$$

$$I_{C2} \left(\frac{1}{\beta} + 1 \right) R_E = V_T \ln \frac{I_{C1}}{I_{C2}}$$

$$R_E = \frac{V_T \beta}{I_{C2} (\beta + 1)} \ln \frac{I_{C1}}{I_{C2}} \quad \text{--- (3)}$$

The Resistance R_E can be adjusted to control the O/p current I_{C2} , here also the I_{ref} is approx. equal to I_{C1} if β is so much greater than 1.

Modified Widlar current source:



Sometimes it is convenient to use R_E in both the transistor Q_1 & Q_2 .
Hence $I_{C1} = I_{C2}$
and the ratio b/w the collector currents is decided by $\frac{I_{C2}}{I_{C1}} \approx \frac{R_1}{R_2}$

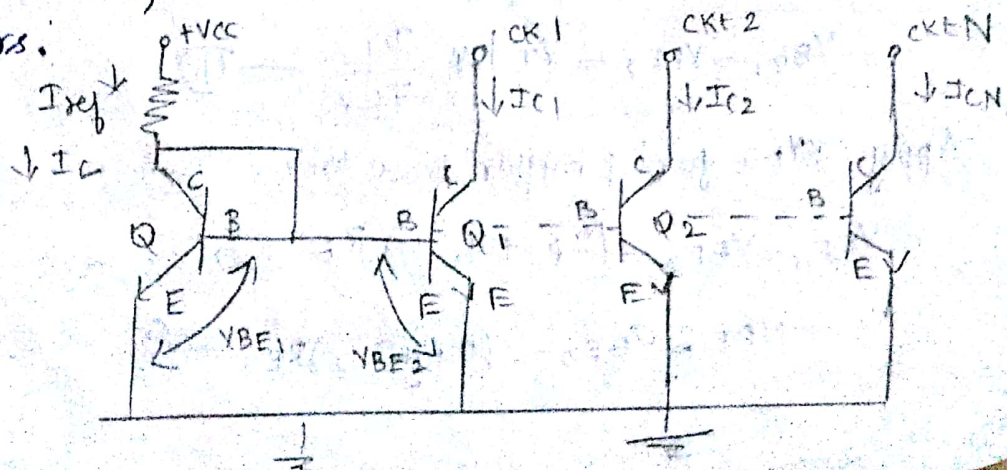
$$\frac{I_{C2}}{I_{C1}} \approx \frac{R_1}{R_2}$$

the ratio that can be practically obtained is b/w

$$0.1 \leq \frac{I_{C2}}{I_{C1}} \leq 10$$

Current Repeaters:

The basic current mirror can be used more than one loads, such a circuit is called current repeaters.

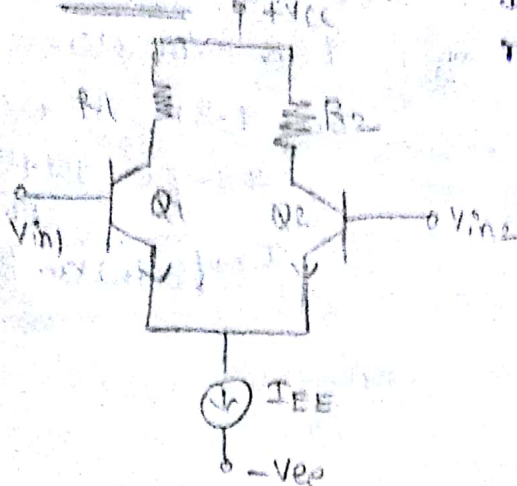


$$I_c = I_{ref} \left[\frac{\beta}{1 + \beta + \beta \cdot \frac{R_1}{R_2}} \right]$$

It is possible to achieve different values of collector currents $I_{c1}, I_{c2}, \dots, I_{cN}$ by scaling the emitter area we can change the current ratio. The same can be achieved by using Widlar current source also,

23/12/17

Problems:



Differential amplifier source resistance of current source is ∞ . The common mode gain is

- a) 0
- b) ∞
- c) indeterminate
- d) $\frac{V_{in1} + V_{in2}}{2V_T}$

2) A Emitter coupled pair of BJT gives linear transfer (only if) V_o and V_{id} . When the magnitude of V_{id} is 4 (b/w) times the thermal voltage

3) (1992) The Differential amp. with CMRR=100 $h_{fe}=100$ $R_E=25\Omega$ at $I_c=1mA$. find the (i) differential gain of the CKE. (ii) common mode gain (iii) find o/p V_o if i/p's are 1010 mV and 990 mV, $R_C=1K\Omega$

$$A_d = g_m \left(\frac{R_C}{2} \right)$$

$$CMRR = \frac{A_{cm}}{A_{cm}}$$

$$r_{\pi} = \frac{\beta V_T}{I_c}$$

$$g_m = \beta / r_{\pi}$$

$$g_m = \frac{I_c}{V_T}$$

$$g_m = \beta \left[\frac{I_c}{V_T} \right]$$

$$g_m = \frac{1 \times 10^{-3}}{26 \times 10^{-3}} = 38.4 m$$

$$= (38.4 \times 10^{-3}) \left(\frac{1K}{2} \right)$$

$$= 19.23$$

$$CMRR = \frac{A_d}{A_{cm}}$$

$$A_{cm} = \frac{19.23}{100} = 0.192$$

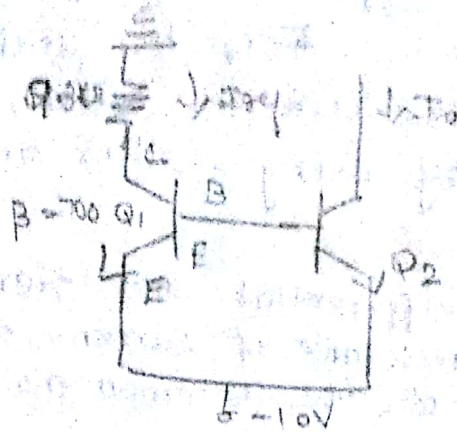
$$V_c = \frac{V_1 + V_2}{2} = 1$$

$$V_d = V_1 - V_2 = 1010 mV - 990 mV = 20 mV$$

$$V_o = \Delta V_d + n V_o$$

$$= 0.576 \Rightarrow 576 \times 10^{-3}$$

4)



Find the value of I_o if the emitter area of Q_1 is half of the Q_2

$$\beta = 115$$

apply KVL

$$I_{ref} \quad 9.3k - V_{BE} + 10 = 0$$

$$I_{ref} \quad 9.3k = 10 + V_{BE}$$

$$I_{ref} = \frac{10 + 0.7V}{9.3k}$$

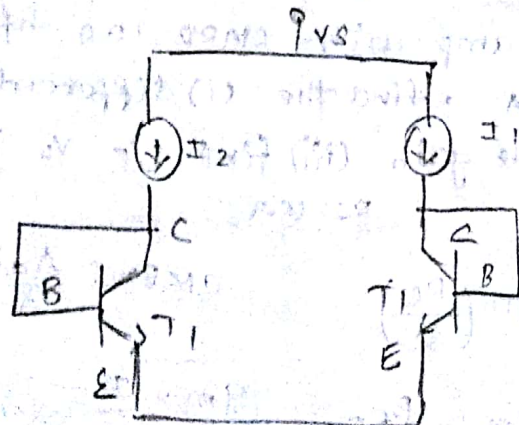
$$I_{ref} = 1.1 \times 10^{-3}$$

$$I_{ref} = 2 I_o$$

$$= 2 \text{ mA}$$

"Q1" is 2 times greater than "Q2"

Q5) In the circuit $I_1 = 80 \text{ mA}$, $I_2 = 4 \text{ mA}$. The transistors are identical $V_T = 26 \text{ mV}$ at 27°C . Find the op V_o which is equal to $V_1 - V_2$ at 50.



$$I/R = V$$

collector base shorted $\rightarrow$ diode

$$273 + 50 = 323$$

$$\frac{I}{11600} = \frac{323}{11600}$$

$$V_T = 27 \text{ mV}$$

$$V_T = 27 \text{ mV}$$

$$I_1 = I_0 \left(e^{V_1 / V_T} \right)$$

$$\frac{I_1}{I_0} = e^{V_1 / V_T} \quad \frac{I_2}{I_0} = e^{V_2 / V_T}$$

Taking ln on both sides

$$\ln \left(\frac{I_1}{I_0} \right) = \frac{V_1}{V_T}$$

$$80 \mu A = I_0 e^{V_1/V_T} ; 4 \mu A = I_0 e^{V_2/V_T}$$

$$\frac{80 \mu A}{4 \mu A} = \frac{I_0 e^{V_1/V_T}}{I_0 e^{V_2/V_T}}$$

$$20 = e^{\frac{V_1 - V_2}{V_T}}$$

$$V_1 - V_2 = \underline{83.28 \text{ mV}}$$

$$\ln(20) = \frac{V_1 - V_2}{V_T}$$

$$\ln(20) \times 27.8 \text{ mV} = V_1 - V_2$$

$$83.28 \times 10^{-3} = V_1 - V_2$$

6) A current mirror provide $1 \mu A$ current for $V_{CC} = 10 \text{ V}$
 $\beta = 125$ $V_{BE} = 0.7 \text{ V}$. Determine R_1
 Find R_1 if I_C is $10 \mu A$

$$I_{ref} = I_C \left[\frac{2 + \beta}{\beta} \right] \Rightarrow 10 \mu \left[\frac{2 + 125}{125} \right] \Rightarrow \underline{10 \mu A}$$

$$I_{ref} = \frac{V_{CC} - V_{BE1}}{R_1}$$

$$R_1 = \frac{V_{CC} - V_{BE1}}{I_{ref}} = \frac{10 - 0.7}{10 \mu A} = \frac{9.3}{10 \mu A} = \underline{930 \text{ K}\Omega}$$

$$\frac{9.3}{10 \times 10^{-3}} = 9.3$$

27/12/17

Replac of R_C :

current source as active loads:

Current source can also be act as a active loads (transistor in place of resistor).

Two requirements are needs

(i) I_0 should be independent of β

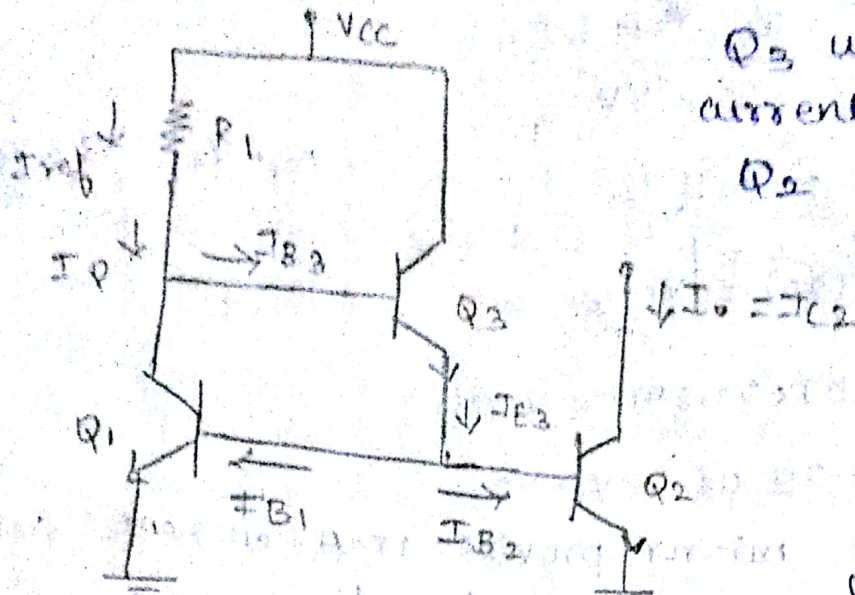
(ii) D/p impedance should be very high to

have high CMRR.

current
source with
gain

wilson
current
source

Current source with gain:



It has a transistor Q_3 which supplies current to Q_1 and Q_2 Base.

for CC configuration

$$\beta = \frac{I_E}{I_B}$$

$$1 + \beta = \frac{I_{E3}}{I_{B3}}$$

$$I_{ref} = I_{C1} + I_{B3}$$

$$= I_{C1} + \frac{I_{E3}}{1 + \beta}$$

$$= I_{C1} + \frac{(I_{B1} + I_{B2})}{1 + \beta}$$

Since the transistor are identical,

$$I_{B1} = I_{B2} = I_B = I_{C1} + \frac{2I_B}{1 + \beta}$$

$$I_B = \frac{I_C}{\beta}$$

$$= I_{C1} + \frac{2I_{C1}}{\beta(1 + \beta)}$$

$$= I_{C1} \left[1 + \frac{2}{\beta^2 + \beta} \right]$$

$$I_{ref} = I_{C1} \left[\frac{\beta^2 + \beta + 2}{\beta^2 + \beta} \right]$$

$$I_O = I_{C1} = I_{ref} \left[\frac{\beta^2 + \beta}{\beta^2 + \beta + 2} \right]$$

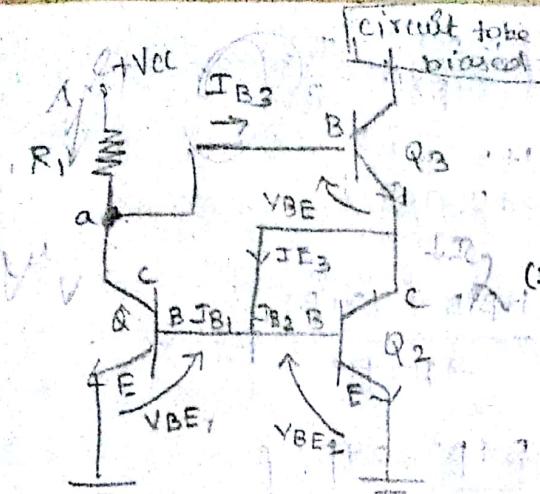
$\beta = 100, 200, 300, \dots, 500$

$$\text{where, } I_{ref} = \frac{V_{CC} - 2V_{BE}}{R_1}$$

Now, the o/p current is independent of

β .

Wilson Current Source:



(1) This current source provides I_o nearly equal to I_{ref} .

(2) It exhibits very high o/p impedance.

The transistors are identical and exhibit $I_{C1} = I_{C2}$

$$\begin{aligned}
 I_{E3} &= I_{C2} + 2 I_{B3} \\
 &= I_{C2} + 2 \frac{I_{C2}}{\beta} \\
 &= I_{C2} \left[1 + \frac{2}{\beta} \right] \\
 &= I_{C2} \left[\frac{\beta + 2}{\beta} \right] = I_{C2} \left[\frac{2 + \beta}{\beta} \right]
 \end{aligned}$$

$$I_{E3} = I_{C2} \left[\frac{2 + \beta}{\beta} \right] \quad \text{--- (1)}$$

$$I_{E3} = I_{B3} + I_{C3} \quad \text{--- (2)}$$

Equate (1) & (2)

$$I_{C2} \left(\frac{2 + \beta}{\beta} \right) = I_{B3} + I_{C3}$$

$$I_{C2} \left(\frac{2 + \beta}{\beta} \right) = \frac{I_{C3}}{\beta} + I_{C3}$$

$$I_{C2} \left(\frac{2 + \beta}{\beta} \right) = I_{C3} \left[\frac{1}{\beta} + 1 \right]$$

$$I_{C2} \left(\frac{2 + \beta}{\beta} \right) = I_{C3} \left[\frac{1 + \beta}{\beta} \right]$$

$$\therefore I_{C3} = I_{C2} \left(\frac{2 + \beta}{1 + \beta} \right) \quad \text{--- (3)}$$

$$\begin{aligned}
 I_o &\simeq I_C \\
 I_{C2} &= I_{C3} \left(\frac{1 + \beta}{2 + \beta} \right)
 \end{aligned}$$

At Node 'A'

apply KVL,

$$\begin{aligned}
 I_{ref} &= I_{C1} + I_{B3} \\
 &= I_{C2} + I_{B3} \quad \text{--- (4)}
 \end{aligned}$$

$$\Rightarrow I_{C3} \left(\frac{1 + \beta}{2 + \beta} \right) + I_{B3}$$

$$= I_{C3} \left(\frac{1+\beta}{2+\beta} \right) + \frac{I_{C3}}{\beta}$$

$$I_{ref} = I_{C3} \left(\frac{1+\beta}{2+\beta} + \frac{1}{\beta} \right)$$

$$I_{ref} = I_{C3} \left[\frac{(1+\beta)\beta + (2+\beta)}{2\beta + \beta^2} \right]$$

$$I_{ref} = I_{C3} \left[\frac{\beta + \beta^2 + 2 + \beta}{2\beta + \beta^2} \right]$$

$$I_{ref} = I_{C3} \left[\frac{\beta^2 + 2\beta + 2}{2\beta + \beta^2} \right]$$

$$I_{C3} = I_{ref} \left[\frac{2\beta + \beta^2}{\beta^2 + 2\beta + 2} \right]$$

Input Resistances:

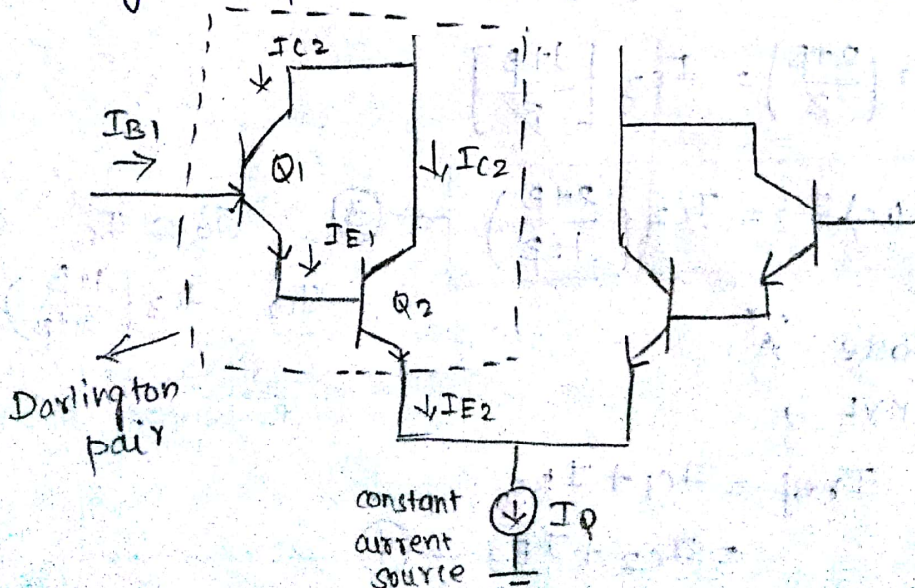
The i/p resistances offered by differential amplifier is called differential input Resistances (R_{id}).

The Resistances R_1, R_2 are floating (not grounded) since R_E is replaced By current source.

The value of $R_{id} = 2h_{ie}$

h_{ie} is i/p resistance of a transistor

To improve the i/p resistance replace Resistances by Darling ton pair (i/p $\uparrow$ impedance) amplifier.



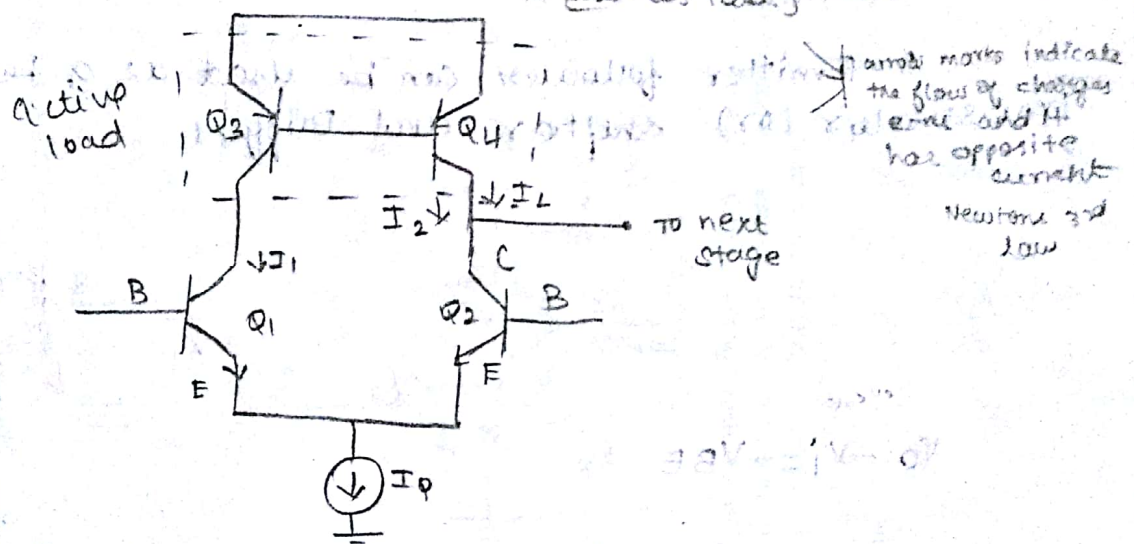
NOTE: Instead of using BJT we can use FET for i/p impedance ($\uparrow$ i/p impedance).

Differential amplifier with active loads:

The load Resistances, R_L can be Replaced by active load but even a cascading of gain stages will achieve infinite gain but this will increase the phase shift and amplifier become unstable (oscillation)

(Observation) To Avoid this we go for active load concept which gives increased gain and increased load resistances.

Now Replace R_C by constant current source using pnp transistors. amplifier $\rightarrow$ npn $\rightarrow$ active component



Under Quiescent condition $V_1 = V_2 = 0$

$$I_1 = I_2 = \frac{I_Q}{2}$$

The load current $I_L = I_1 - I_2 = 0$

Assume

(i) $V_1 > V_2$, then $I_t = I_1 - I_2$
 $= qnV_1 - qnV_2$

$$V_1 - V_2 = V_d$$

$$I_L = gm(V_1 - V_2)$$

$$I_t = qmV_d$$

Note:

The ckt acts as a transconductance amplifier.

Level Translator and Buffer - temporarily if stores
 It (as as impedance matching)

Level Translator (or) Level Shifter:

It is used to

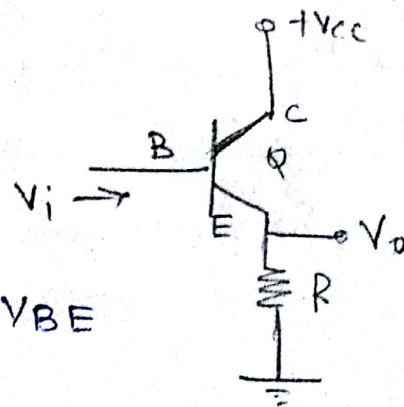
(i) Direct coupling (no coupling capacitors are their. Hence the dc level rises from stage to stage which shift the

(ii) For '0' i/p o/p be '0' (active) P-point which will result in distortion

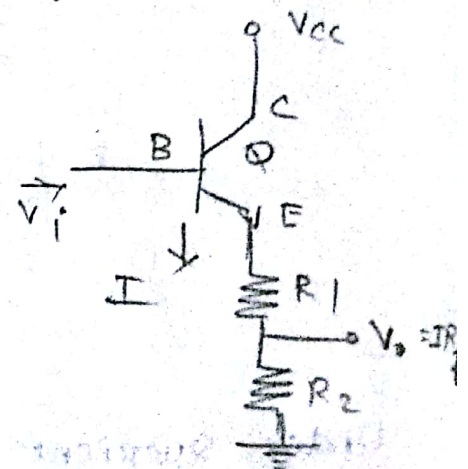
Impedance matching should be done

[Differential amp o/p Impedance is ∞ , External Load i/p Impedance is $\downarrow$, so there will be impedance mismatch) Hence Buffer be connected which connect high impedance to low impedance.

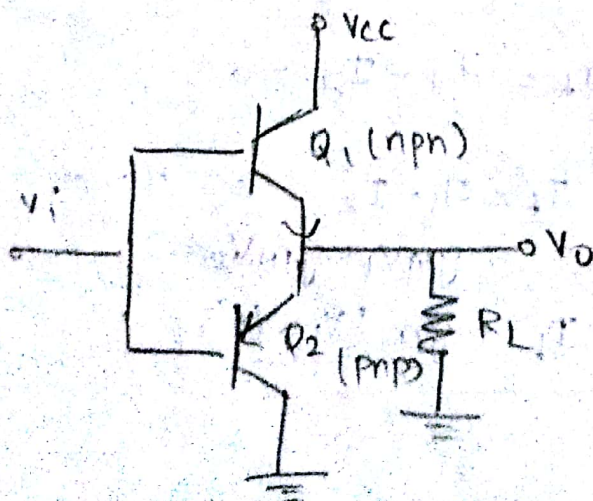
A Emitter follower can be used as a Level Translator (or) shifter and Buffer.



$$V_o - V_i = -V_{BE}$$

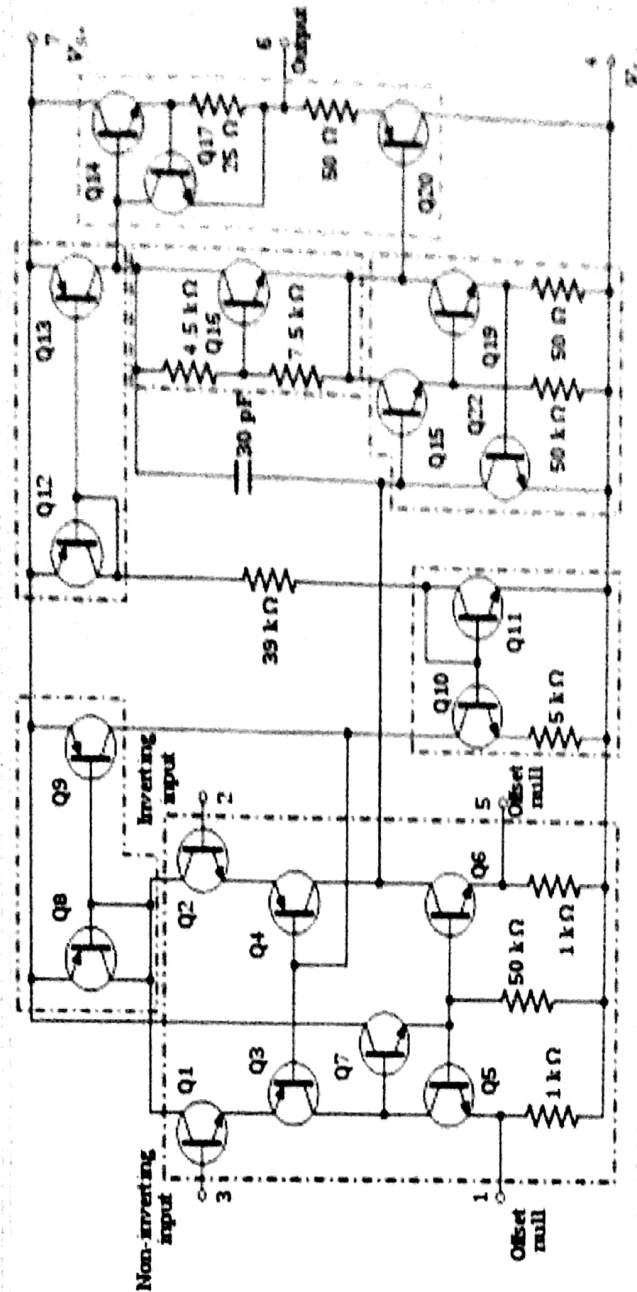


output stage:



28/12/11

Internal circuitry of 741-type op-amp



A component-level diagram of the common 741 op-amp. Dotted lines outline: current mirrors (red); differential amplifier (blue); class A gain stage (magenta); voltage level shifter (green); output stage (cyan).

Explanation:

The input stage consists of Q_1, Q_3, Q_2, Q_4 - It is a cascode stage (CE, CB)

Q_5, Q_6, Q_7 - It is a active load for Q_3, Q_4 of Q_5, Q_6 is a differential amplifier.

$(Q_8, Q_9), (Q_{10}, Q_{11}), (Q_{12}, Q_{13})$ forms the current mirror.

(Q_5, Q_{19}, Q_{22}) forms the gain stage using class A amplifier.

Q_{16} forms the voltage level shifter which controls the DC bias shifting.

(Q14, Q20, Q17) forms the output stage which delivers the op-amp output which forms a complementary symmetry pair.
 (high switching capability)

A 30pF capacitor is provided high frequency to stabilize the circuit.
 (roll off)

Offset Null is provided by R51Q6 which can be obtained by externally connecting 10K Ω potentiometer.
 (we can eliminate by adjusting this)

Performance characteristics of an op-amp:
 (only AC) op-amp work on both AC & DC.
 (both AC & DC)

DC characteristics:

An ideal op-amp draws no current and its response is independent of temperature.
 (25mV waste during 180 $^\circ$ it doubles in 180 $^\circ$)

Where practically these assumptions are not applicable due to transistor mismatch conduction and β i/p's (IV and NIV) Respond differently all the time.

These reasons create an error components for DC voltages and these are called DC characteristics.

Name of DC characteristics:

- * Input bias current
- * Input offset current
- * Input offset voltage
- * Thermal drift

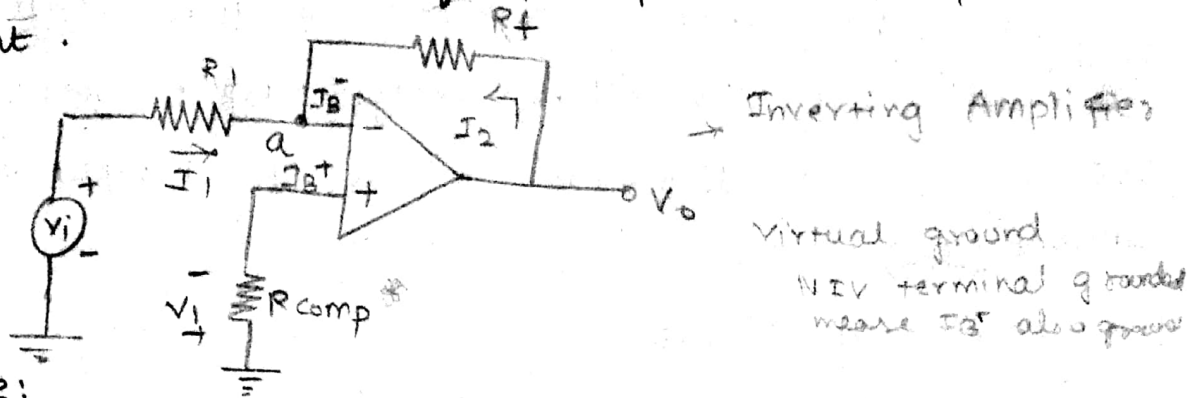
1) Input bias current:

The op-amp made of BJT is biased in the linear region by supplying current into the bases (Biasing).

We also assume. 0 $^\circ$ current is drawn by the op-amp. Hence ideally no shift in the Q-point. There will be some base current I_{B^+} , I_{B^-} are not equal due to internal imbalanced.

This current is called input bias current.

The Average value of base current entering into I_N and I_{IV} terminals of op-amp is called input bias current.



Note:

Since op-amp draws no current if non-inverting terminal is grounded. When the I_V terminal node a is also considered as grounded, this is known as virtual ground concept in op-amp.

$$\text{input bias current } \left\{ \begin{array}{l} I_B = \frac{I_B^+ + I_B^-}{2} \end{array} \right.$$

If $V_i = 0$, then $V_o = 0$ but because of this bias current $V_o \neq 0$.

$$\text{i.e.) in IC 741 } \left\{ \begin{array}{l} I_B = 500 \text{ nA} \quad \text{BJT op-amp} \\ R = 1 \text{ M}\Omega \end{array} \right.$$

$$V_o = R I_B = 10^6 \times 500 \times 10^{-9} = 500 \times 10^{-9} \times 10^6$$

$V_o = 0.5 \text{ V}$ which is supposed to be "zero".

$$\begin{aligned} I_B &= I_1 + I_2 \\ &= \frac{V_i}{R_i} + \frac{V_i}{R_f} \\ &= V_i \left[\frac{1}{R_i} + \frac{1}{R_f} \right] \end{aligned}$$

$$I_B = V_i \left[\frac{R_f + R_i}{R_i R_f} \right]$$

$$\therefore R_{comp} = R_f \parallel R_i$$

$$\frac{V_o}{R_f} = \frac{V_i}{R_i}$$

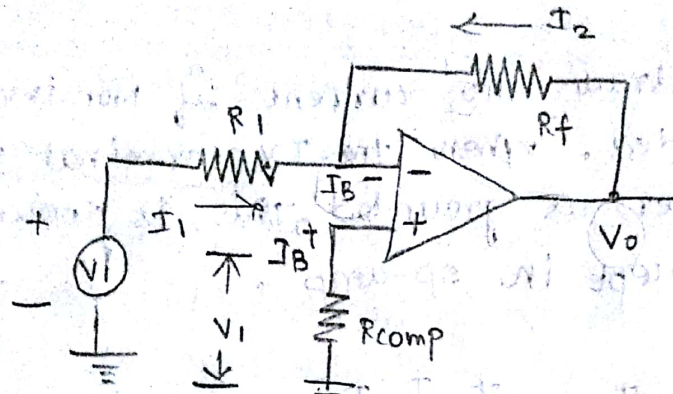
R_{comp} is to overcome the i/p bias current.

3/1/18

Input offset current

The Bias current compensation work only if $I_B^+ = I_B^-$, But their will be small output voltage due to I_B^+ , I_B^- difference this is called input offset current (I_{os})

consider a circuit,



Analysis:

$$V_1 = I_B^+ R_{comp} \quad \text{--- (1)}$$

$$I_B^- = I_1 + I_2 \quad \text{--- (2)}$$

$$I_2 = I_B^- - I_1$$

$$= I_B^- - V_1 / R_1 \quad \text{--- (3)}$$

sub (1) in (3)

$$I_2 = I_B^- - \frac{I_B^+ R_{comp}}{R_1} \quad \text{--- (4)}$$

$$V_o = I_2 R_f - V_1 \quad \text{--- (5)}$$

sub (4) in (5)

$$\Rightarrow R_f \left(I_B^- - \frac{I_B^+ R_{comp}}{R_1} \right) - (I_B^+ R_{comp})$$

$$R_{comp} = \frac{R_1 R_f}{R_1 + R_f}$$

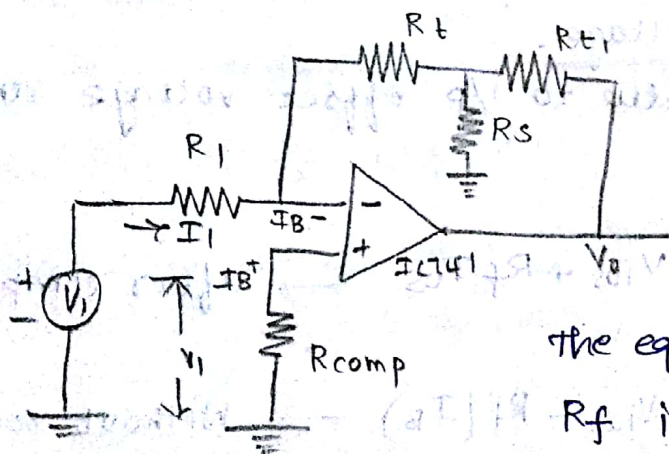
$$R_f \left[I_B^- - I_B^+ \left(\frac{R_1 R_f}{R_1 + R_f} \right) \right] - \left[I_B^+ \left[\frac{R_1 R_f}{R_1 + R_f} \right] \right]$$

$$\begin{aligned}
 &= R_f \left[I_B^- - I_B^+ \left(\frac{R_f}{R_i + R_f} \right) \right] - \left[I_B^+ \frac{R_i R_f}{R_i + R_f} \right] \\
 &= R_f \left[I_B^- - \frac{I_B^+ R_f}{R_i + R_f} - \frac{I_B^+ R_i}{R_i + R_f} \right] \\
 &= R_f \left[I_B^- - I_B^+ \left(\frac{R_f}{R_i + R_f} + \frac{R_i}{R_i + R_f} \right) \right] \\
 &= R_f \left[I_B^- - \frac{I_B^+}{R_i + R_f} (R_f + R_i) \right]
 \end{aligned}$$

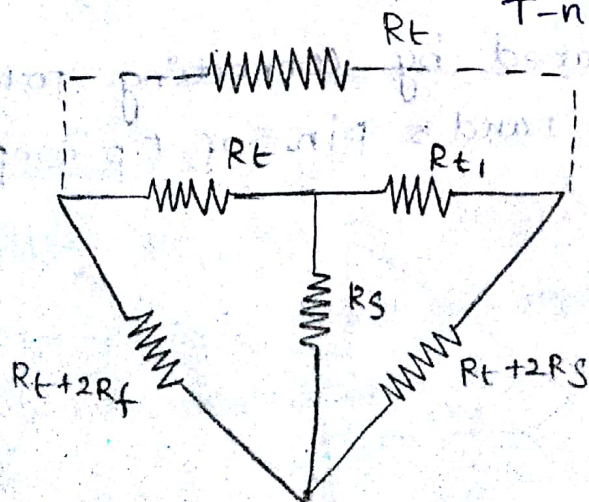
$$V_o = R_f (I_B^- - I_B^+)$$

The o/p voltage V_o depend on the input offset current $[R_f \times I_{os}]$

TO overcome this, a T- network is used in the feedback,



the equation for calculating R_f is done by converting T-network into π -network

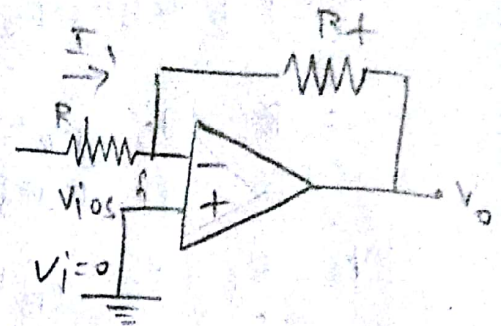
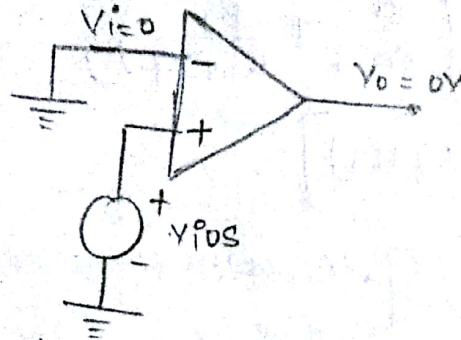


$$R_f = \frac{R_t^2 + 2R_t R_s}{R_s}$$

For practical design (R_t should be so much less than R_f) $R_t \ll R_f/2$

INPUT OFFSET VOLTAGE

In spite of above compensation, the o/p may not be equal to 0, for input '0' v.tg. To nullify this a small voltage V_{ios} is given to the op-amp.



V_{ios} is applied
 a Non-inverting terminal of op-amp.

$$V_o = \left[1 + \frac{R_f}{R_i} \right] V_{ios}$$

DRB Rheostat

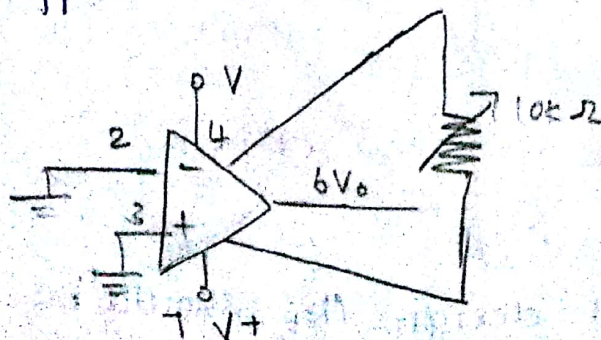
Total offset o/p voltage.

This is due to i/p offset voltage and
 i/p bias current.

$$V_o = \left[1 + \frac{R_f}{R_i} \right] V_{ios} + R_f I_{os} \rightarrow \text{after compensation}$$

$$= \left[1 + \frac{R_f}{R_i} \right] V_{ios} + R_f (I_B) \rightarrow \text{Without compensation}$$

This can be eliminated by connecting potentiometer (10k Ω) b/w or across 1 and 5 pin of op-amp to nullify this effect.



Thermal drift

The bias current, offset current and offset voltage change with temperature even after compensation. The change in these characteristics with respect to temperature is called thermal drift.

Causes:

(1) This can be avoided by proper selection of PCB.

(2) Keeping the op-amp away from the PCB and air cooling be provided

Note: $\frac{1}{p}$ ut, offset current & offset voltage, thermal drift
DC characteristics affect only steady state response. (only DC i/p) AC - small signal analysis

4/1/18

AC Performance characteristics

The 3 components be affected by AC characteristics

1) Frequency response

3) Slew Rate.

2) stability of op-amp

Frequency $\rightarrow$ To find operating range of op-amp (or frequency)



convert to dB means that be 3dB

Bandwidth

low pass filter

freq. $f = 0 - 10$ Hz

Application $\rightarrow$ Radio

$$f = \frac{1}{2\pi RC}$$

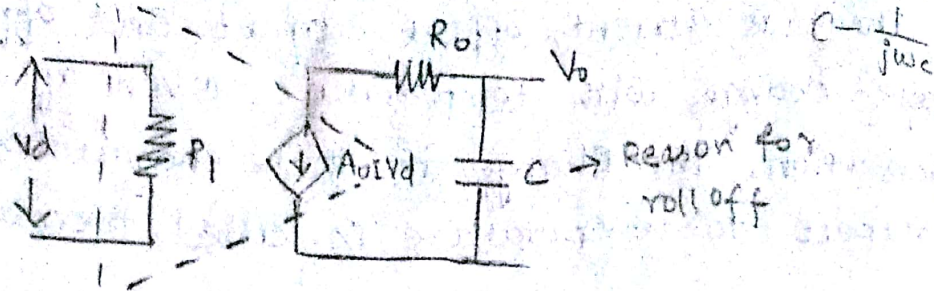
1) Frequency Response:

1) Ideally op-amp has infinite bandwidth

ie) through out audio to radio frequency range bandwidth should be same.

2) As frequency increases roll off occurs which limits the bandwidth. Due to the capacitance effect which occurs in the BJT. (Inter electrode capacitance)

Hence equivalent circuit is modified as



$$V_o = A_{OL} V_d \frac{C}{R_o + C}$$

$$V_o = A_{OL} V_d \frac{1/j\omega C}{R_o + \frac{1}{j\omega C}}$$

$$\omega = 2\pi f$$

$$f_1 = \frac{1}{2\pi R_o C}$$

$$V_o = A_{OL} V_d \frac{1}{\frac{2\pi f}{R_o + \frac{1}{2\pi f C}}}$$

$$V_o = A_{OL} V_d \frac{1/j\omega C}{R_o + \frac{1}{j\omega C}}$$

$$A_{OL} V_d \frac{1}{\frac{2\pi f}{(R_o 2\pi f C + 1)}}$$

$$= A_{OL} V_d \frac{1}{1 + j R_o \omega C}$$

$$= A_{OL} V_d \frac{1}{1 + j 2\pi f R_o C}$$

$$A_{OL} V_d \left(\frac{1}{2\pi f} \times \frac{2\pi f C}{(f_1 + 1)} \right)$$

$$= A_{OL} V_d \frac{1}{1 + j f/f_1}$$

$$V_o = A_{OL} V_d \left(\frac{C}{(f_1 + 1)} \right)$$

$$\frac{V_o}{V_d} = \frac{A_{OL} C}{1 + j f/f_1}$$

$$V_o = A_{OL} V_d C f_1$$

$$A = \frac{A_{OL} C}{1 + j f/f_1}$$

The open loop gain decreases by factor $1 + j f/f_1$, which is due to the capacitance effect.

5/1/18

$$A_{OL} = \frac{1}{1 + j f/f_1}$$

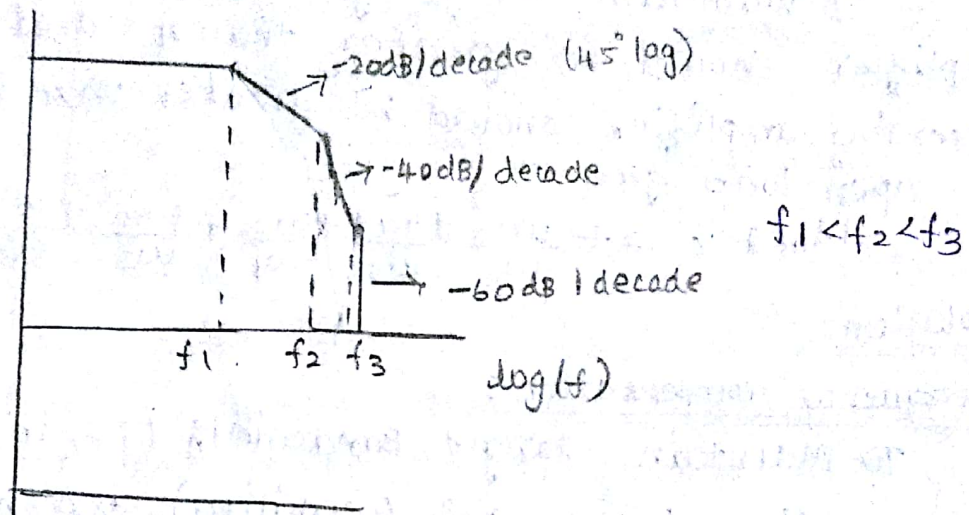
$$|A_{OL}| = \frac{1}{\sqrt{1 + (f/f_1)^2}}$$

$$|a + jb| = \sqrt{a^2 + b^2}$$

If we have more than 1 cut off frequency then the gain and close loop gain.

Close loop gain:

$$A = \frac{A_{o1}}{(1+jf/f_1)(1+jf/f_2)(1+jf/f_3)}$$



Since Op-amp has no. of stages each stage will contribute capacitor 'C' there will be more than one corner frequency f_1, f_2, f_3 .

Note:

One corner frequency contribute -20dB/decade roll off with the lag of 45° phase angle.

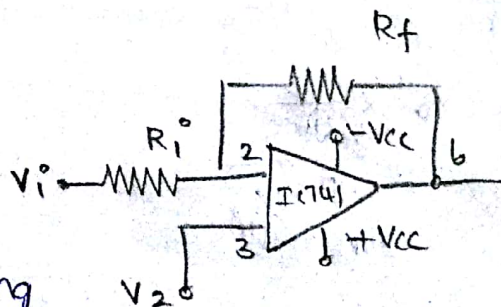
II STABILITY OF OP-AMP:

↓ (obey the order)

Amplifier

$$|A\beta| = 1$$

For inverting



amplifier there will be 180° phase shift because of the capacitance effect with more than 2 corner frequency provide another 180° phase shift, so totally $180 + 180 = 360^\circ$ the closed loop gain of amplifier is,

$$A_{cl} = \frac{A}{1+A\beta}$$

$1+A\beta = 0$ is the characteristic equation

$$A\beta = -1$$

$$|A\beta| = 1$$

Hence both the condition for sustain oscillation is obtain hence the amplifier break into oscillation causing instability.

To maintain stability the gain of inverting amplifier should be greater than 4 and non-inverting amplifier should be greater than 5, and the open loop gain

$$|A_{OL}| < 2 + \frac{\omega_1}{\omega_2} + \frac{\omega_1}{\omega_3} + \frac{\omega_2}{\omega_1} + \frac{\omega_2}{\omega_3} + \frac{\omega_3}{\omega_1} + \frac{\omega_3}{\omega_2}; \beta = 1$$

Solution:

Frequency compensation:

To maintain larger Bandwidth (i.e., in freq response) and low closed loop gain (stability) we need compensation technique.

1) External
 $\swarrow$ dominant pole
 $\searrow$ pole-zero

2) Internal

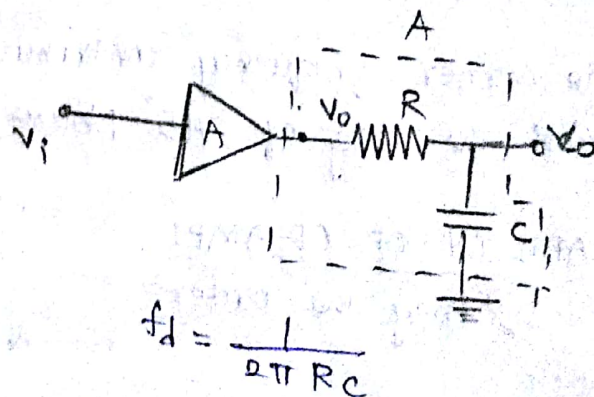
$$A' = AA_1'$$

$$V_o = V_o' \times \frac{1}{\frac{R + 1/j\omega C}{j\omega C}}$$

$$V_o = V_o' \times \frac{1}{\frac{j\omega RC + 1}{j\omega C}}$$

$$= \frac{1}{1 + j2\pi f RC}$$

$$A' = \frac{1}{1 + jf/f_d} \quad \text{--- ①}$$

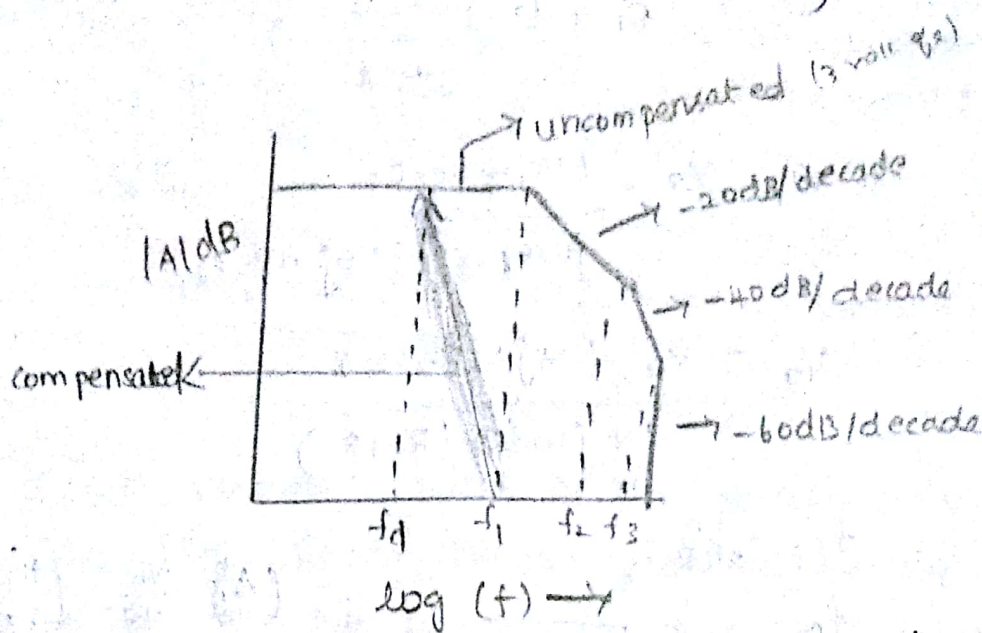


$$f_d = \frac{1}{2\pi RC}$$

$$V_o = \frac{V_o'}{j\omega RC + 1}$$

$$\frac{V_o}{V_o'} = \frac{1}{j\omega RC + 1}$$

$$A = \frac{A_{OL}}{(1+jf/f_1)(1+jf/f_2)(1+jf/f_3)} \quad (2)$$



The capacitor 'c' in the dominant pole (network) selected such that ^{loop gain} drops to 0 (degree) dB with slope of -20 dB/decade at f_1 .

Advantages:

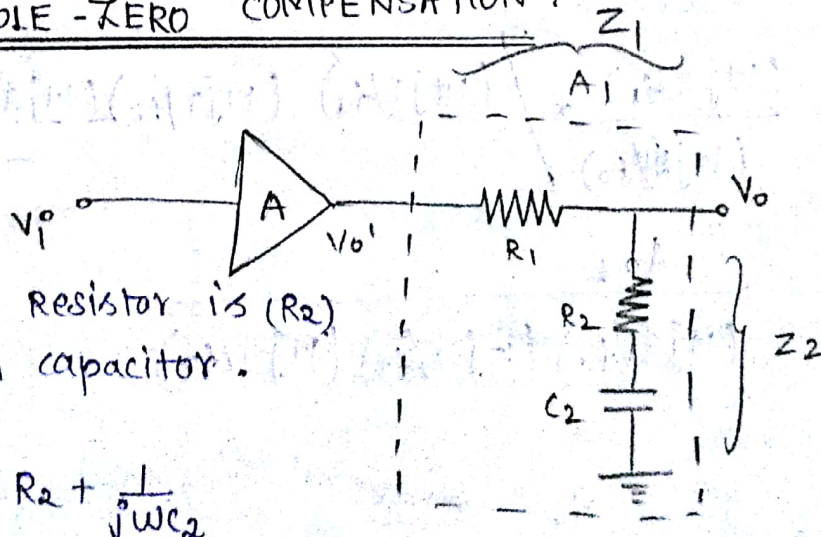
Noise immunity is better

Disadvantage:

gain $\downarrow$ drastically with lesser BW

6/1/18

POLE-ZERO COMPENSATION:



An Extra Resistor is (R_2) added with capacitor.

$$Z_2 = R_2 + \frac{1}{j\omega C_2}$$

$$Z_2 = \frac{1 + R_2 j\omega C_2}{j\omega C_2}$$

$$V_o = V_o' \times \frac{Z_2}{Z_1 + Z_2} \quad \text{voltage division rule.}$$

$$V_o = V_{o1}' \times \frac{1 + j\omega R_2 C_2}{j\omega C_2} \cdot \frac{j\omega C_2}{R_1 + (1 + j\omega R_2 C_2)}$$

$$(V_o) = V_{o1}' \cdot \frac{(1 + j\omega R_2 C_2)}{j\omega R_1 C_2 + (1 + j\omega R_2 C_2)}$$

$$V_o = V_{o1}' \frac{(1 + j\omega R_2 C_2)}{1 + j\omega C_2 (R_1 + R_2)}$$

$$\omega = 2\pi f$$

$$f_1 = \frac{1}{2\pi R_2 C_2}$$

$$f_0 = \frac{1}{2\pi (R_1 + R_2) C_2}$$

$$(A_1)' = \frac{V_o}{V_{o1}'} = \left(\frac{1 + jf/f_1}{1 + jf/f_0} \right)$$

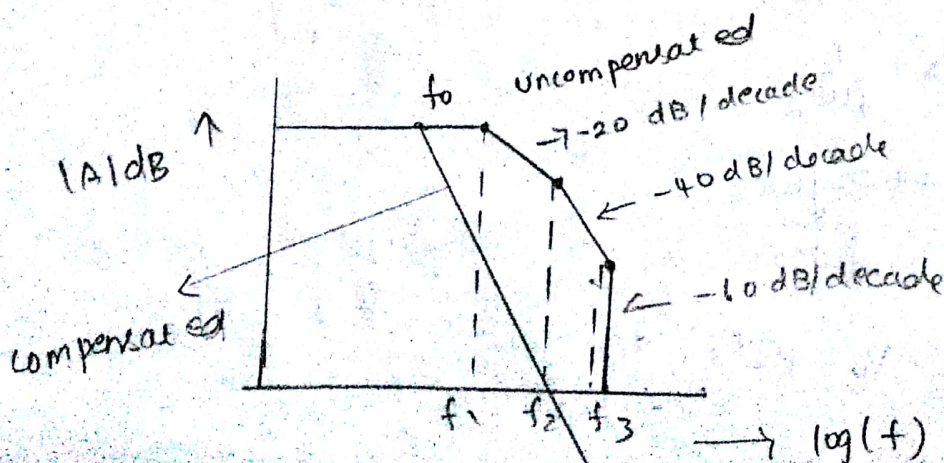
$$V_o = V_{o1}' \frac{(1 + j2\pi f_1)}{(1 + j2\pi f_0)} = V_{o1}' \frac{(1 + jf/f_1)}{(1 + jf/f_0)}$$

$$A = \frac{A_{OL}}{(1 + jf/f_1)(1 + jf/f_2)(1 + jf/f_3)} \quad f_1 \rightarrow \text{eliminated}$$

$$A' = A_1 A$$

$$A' = \frac{(1 + jf/f_1)}{(1 + jf/f_0)} \times \frac{1}{(1 + jf/f_1)(1 + jf/f_2)(1 + jf/f_3)}$$

$$A' = \frac{A_{OL}}{(1 + jf/f_0)(1 + jf/f_2)(1 + jf/f_3)}$$



Internally compensated op-Amp:

An internal capacitance of 10 pF to 20 pF connected b/w i/p and o/p stage which provides compensation. This is called Miller effect compensation.

2nd SLEW RATE: freq-speed

Rise time is the time taken by the o/p to change from 10% - 90% of final value. BW ↑ tr ↓

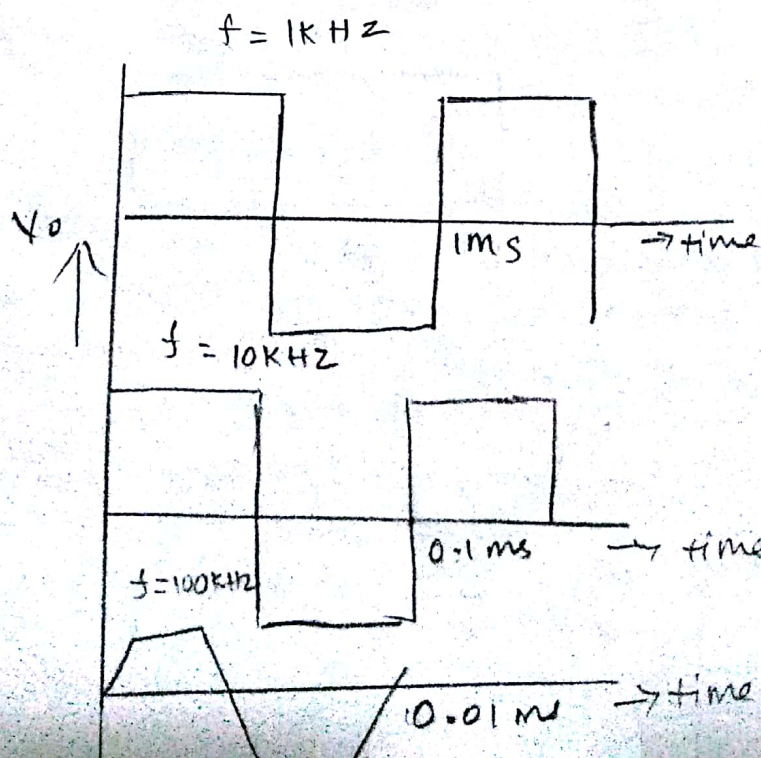
$$t_r = \frac{0.35}{BW}$$

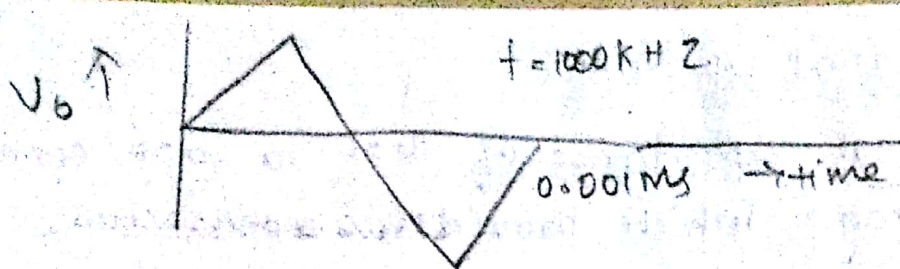
Ideal response time of the op-amp should be 0. O/p v_{tg} should respond instantaneously to any change in i/p. But practically this is possible for small signal.

For large signal the op-amp speed is limited and it is measured in terms of slew rate which is defined as "Maximum rate of change of v_{tg} caused by step i/p v_{tg} ".

$$SR = \frac{I_{max}}{C} \Rightarrow \frac{2\pi f V_m}{10^6} \text{ V}/\mu\text{s}$$

f is the full power response of a large signal of which op-amp gives the o/p ^{with out} distortion.

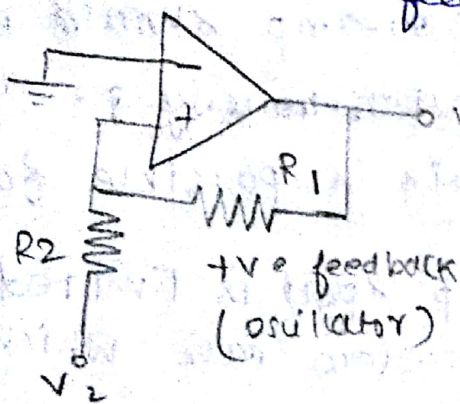




Open and close loop configuration of op-amp.

Op-amp can be operated at both open loop (without feedback), closed loop (with feedback).

In closed loop, gain of the op-amp is obtained and Resistor, ^{wire (voltage follower)} is connected b/w (Pin 6 and 2) -ve feedback to provide -ve feedback (necessary cond. for ^{to prov} amplification)



In open loop, there is no feedback b/w pin 6 and 2 (and) +ve feedback b/w pin 6 and 3. Always

O/p be square wave with amplitude $\pm V_{sat}$ (decided by the V_{cc})

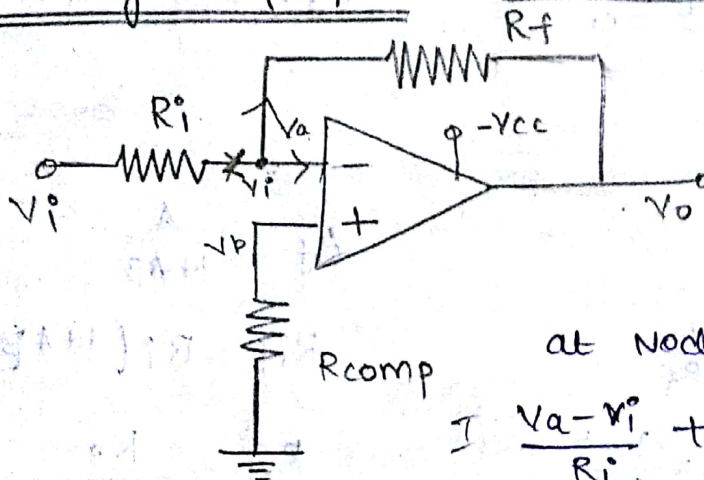
I CLOSE LOOP APPLICATION:Linear applications:

- 1) Adder
- 2) Subtractor
- 3) V-I converter
- 4) I-V converter
- 5) Instrumentation amplifier
- 6) Integrator
- 7) Differentiator

NON-Linear application

- 1) Rectifier
- 2) Peak detector
- 3) Clipper
- 4) clamper
- 5) log, Anti log amplifier.

8/11/18

Inverting amplifier: (180° phase shift and provide gain)

- (1) It will provide 180° phase shift
- (2) And also provide a gain 'A'.

at Node 'A' apply KCL

$$\therefore \frac{V_a - V_i}{R_i} + \frac{V_a - V_o}{R_f} = 0 \quad \text{--- (1)}$$

By virtual ground concept $V_b = 0$ hence $V_a = 0$
 sub in equ (1)

$$-\frac{V_i}{R_i} - \frac{V_o}{R_f} = 0$$

$$V_o = -\frac{R_f}{R_i} V_i$$

$$\frac{V_o}{R_f} = -\frac{V_i}{R_i}$$

$$V_o = -R_f \frac{V_i}{R_i}$$

$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_i}$$

(close loop gain of the inverting amplifier)

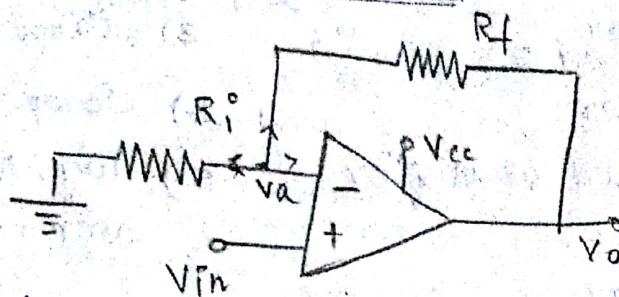
but practically due to -ve feedback every parameter varies.

$$A_f = \frac{A}{1 + A\beta} \quad (\text{feedback gain})$$

(1/p resistance R_{if} with feedback) $= R_i + \frac{R_f}{1+A}$ || R_{in}

$$R_{of} = \frac{R_o}{1+A\beta}$$

Non-Inverting Amplifiers:



No phase shift,
but close loop
gain is then.

@ node A, Apply KCL,

$$\frac{V_a - 0}{R_i} + \frac{V_a - V_o}{R_f} = 0$$

$$\boxed{V_a = V_i}$$

$$A_{CL} = \frac{V_o}{V_i} = \frac{V_a}{V_i} + \frac{V_a - V_o}{V_i} \cdot \frac{R_f}{R_i}$$

$$A_f = \frac{A}{1+A\beta}$$

$$A_{CL} = \frac{V_o}{V_i} + \frac{V_i}{V_i} \cdot \frac{R_f}{R_i} = \frac{V_o}{V_i} + \frac{R_f}{R_i}$$

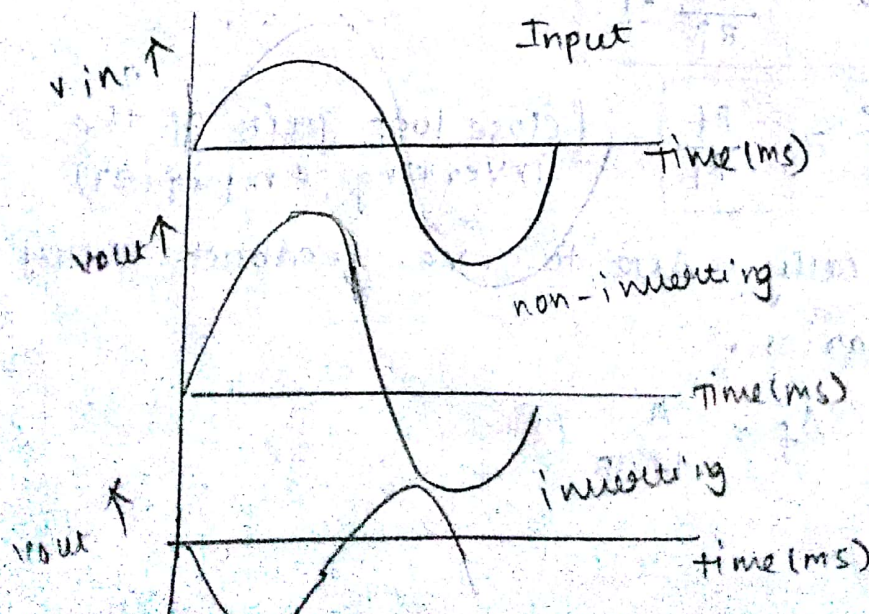
$$R_{if} = R_i (1+A\beta)$$

$$V_i \left(\frac{1}{R_i} + \frac{1}{R_f} \right) = \frac{V_o}{R_f}$$

$$R_{of} = \frac{R_o}{1+A\beta}$$

$$V_i \left(\frac{R_i + R_f}{R_i R_f} \right) = \frac{V_o}{R_f}$$

$$\boxed{A_{CL} = V_i \left(1 + \frac{R_f}{R_i} \right)}$$



note: calculate A_f , R_{if} , R_{of} for inverting op-amp specification.
 given R_i , R_f A - open loop gain
 Open loop gain (A) is 20,000. input impedance
 $R_{in} = 2M\Omega$, $R_o = 75\Omega$.

β = feedback factor

$$\beta = \frac{R_i}{R_i + R_f}$$

Scale changer/sign changer (inverter) $\rightarrow$ (only sign changer) equal
 $\rightarrow$ changing only amplitude $i/p = 1$ $o/p = -1$ ($R_i = R_f$)
 (INV)

signchanger $\rightarrow$ analog inverter

$\rightarrow$ apply $\rightarrow$ 7405 -ve regulator
 we can use this

scale changer:

It is a normal inverting amplifier which changes the magnitude of the input.

$$\frac{R_f}{R_i} = k$$

sign changer:

It changes only the phase of the input.

$$\frac{R_f}{R_i} = -1$$

It is also called as Inverter.

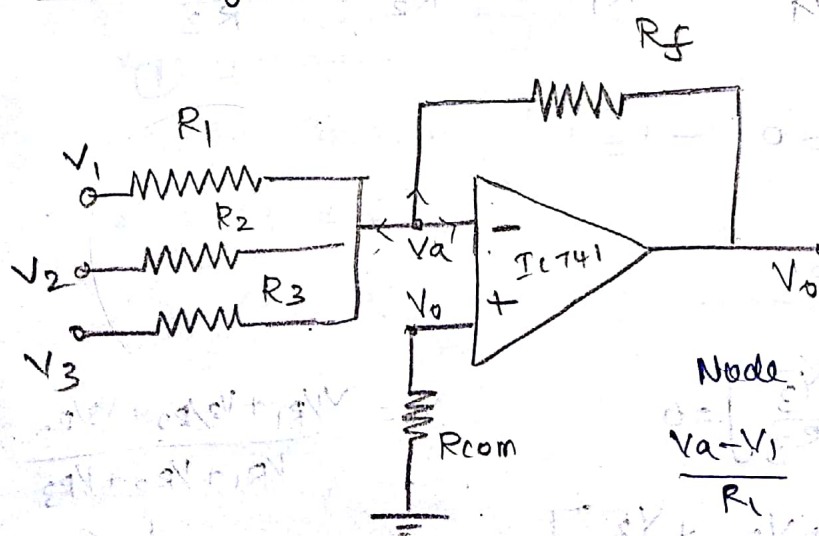
summing amplifier/adder:

The o/p is sum of several input voltage.

Types of adder;

- (i) Inverting adder
- (ii) Non-Inverting adder

Inverting adder:



$$R_{comp} = R_i \parallel R_f = R_1 \parallel R_2 \parallel R_3 \parallel R_f$$

we can give either AC or DC as a i/p.

Node analysis,

$$\frac{V_a - V_1}{R_1} + \frac{V_a - V_2}{R_2} + \frac{V_a - V_3}{R_3} + \frac{V_a - V_o}{R_f} = 0$$

$$V_a = 0$$

$$\frac{-V_1}{R_1} - \frac{V_2}{R_2} - \frac{V_3}{R_2} = \frac{V_0}{R_f}$$

$$V_0 = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

$$R_f = R_1 = R_2 = R_3 = R$$

$$V_0 = -R \left(\frac{V_1 + V_2 + V_3}{R} \right)$$

$$V_0 = -(V_1 + V_2 + V_3)$$

adder

$$R_1 = R_2 = R_3 = 3R_f$$

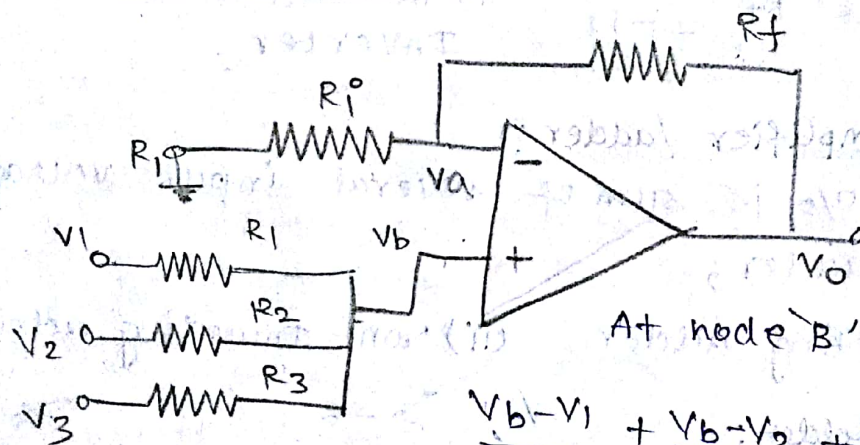
$$V_0 = -R_f \left(\frac{V_1 + V_2 + V_3}{3R_f} \right)$$

$$V_0 = \frac{V_1 + V_2 + V_3}{3}$$

— Average

9/11/18

NON-Inverting adder:



At node 'B'.

$$\frac{V_b - V_1}{R_1} + \frac{V_b - V_2}{R_2} + \frac{V_b - V_3}{R_3} = 0 \quad \text{--- (1)}$$

At node 'A'.

$$\frac{V_a}{R_i} + \frac{V_a - V_0}{R_f} = 0 \quad \text{--- (2)}$$

from eqn (1) $V_a = V_b$

$$V_b \left[\frac{-V_1}{R_1} - \frac{V_2}{R_2} - \frac{V_3}{R_3} \right] = 0$$

$$V_b = \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right]$$

$$V_b = \frac{V_1/R_1 + V_2/R_2 + V_3/R_3}{1/R_1 + 1/R_2 + 1/R_3} \quad \text{--- (1)}$$

At node a: $\frac{V_a}{R_i} + \frac{V_a - V_o}{R_f} = 0$

$$V_a \left(\frac{1}{R_i} + \frac{1}{R_f} \right) = \frac{V_o}{R_f}$$

$$V_a = V_b$$

$$\frac{V_o}{R_f} = V_b \left(\frac{1}{R_i} + \frac{1}{R_f} \right) = \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right) \left(\frac{1}{R_i} + \frac{1}{R_f} \right)$$

$$V_o = \frac{\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)}{\frac{1}{R_i} + \frac{1}{R_f}} \left(\frac{R_i + R_f}{R_i R_f} \right) R_f$$

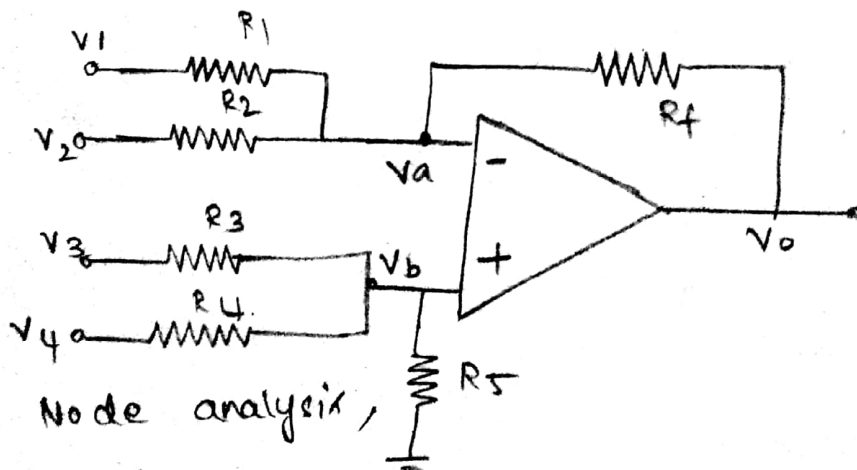
$$V_o = \left(1 + \frac{R_f}{R_i} \right) \left(\frac{V_1/R_1 + V_2/R_2 + V_3/R_3}{1/R_i + 1/R_f} \right)$$

$$R_f = R_i = R$$

$$V_o = 2 \left(\frac{V_1/R_1 + V_2/R_2 + V_3/R_3}{1/R_i + 1/R_f} \right)$$

Adder / subtractor:

$$V_i = V_b$$



Node analysis,

At node B,

$$\frac{V_b - V_3}{R_3} + \frac{V_b - V_4}{R_4} = 0 \quad \text{--- (1)}$$

at node A,

$$\frac{V_a - V_2}{R_2} + \frac{V_a - V_1}{R_1} + \frac{V_a - V_o}{R_f} = 0 \quad \text{--- (2)}$$

from ①

$$V_b \left[\frac{-V_3}{R_3} - \frac{V_4}{R_4} \right] = 0$$

$$V_b = \frac{V_3}{R_3} + \frac{V_4}{R_4}$$

$$V_b = \left[\frac{V_3/R_3 + V_4/R_4}{1/R_3 + 1/R_4 + 1/R_5} \right]$$

from equ ②

$$V_a \left[\frac{-V_1}{R_1} - \frac{V_2}{R_2} - \frac{V_0}{R_f} \right] = 0$$

$$V_a = \frac{\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} \right) + \frac{V_0}{R_f}}{1/R_1 + 1/R_2 + 1/R_f}$$

$$V_a = V_b$$

$$\frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_0}{R_f}}{1/R_1 + 1/R_2 + 1/R_f} = \frac{V_3/R_3 + V_4/R_4}{1/R_3 + 1/R_4 + 1/R_5}$$

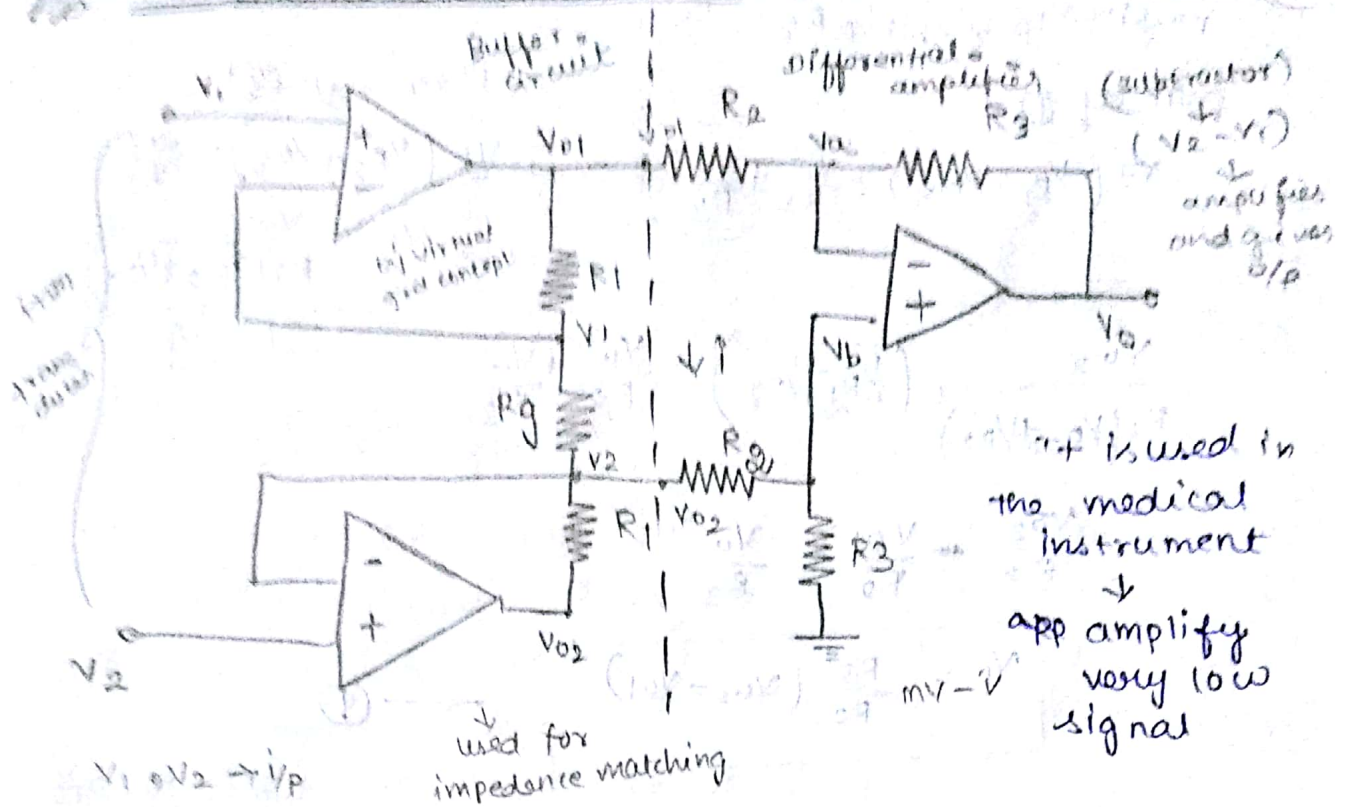
$$R_1 = R_2 = R_3 = R_4 = R_f = R$$

$$\frac{\frac{V_1 + V_2 + V_0}{R}}{(3/R)} = \frac{\left(\frac{V_3 + V_4}{R} \right)}{(3/R)}$$

$$V_1 + V_2 + V_0 = V_3 + V_4$$

$$V_0 = (V_3 + V_4) - (V_1 + V_2)$$

Instrumentation Amplifier:



* This amplifier measures even small signal from transducers (is a sensor) (converts physical quantities light, temperature from sensor into electrical signals).

* It is a kind of differential amplifier outfitted with buffer circuit for impedance matching.

* It measures the signal of interest and eliminates the common mode signal (noise) since it has high CMRR.

Features:

- ① Very low dc offset
- ② Low thermal drift
- ③ Very high CMRR
- ④ Very high i/p impedance
- ⑤ Very high open loop gain.

Analysis:

(1) In a Differential amplifier part,

Apply node equation,

$$\frac{V_a - V_{o1}}{R_2} + \frac{V_a - V_o}{R_3} = 0 \quad \text{--- (1)}$$

$$\frac{V_b - V_{o2}}{R_2} + \frac{V_b}{R_3} = 0 \quad \text{--- (2)}$$

from eq ①

$$V_a \left(\frac{1}{R_1} + \frac{1}{R_3} \right) = \frac{V_{o1}}{R_2} + \frac{V_o}{R_3}$$

From eqn ②

$$V_b \left(\frac{1}{R_2} + \frac{1}{R_3} \right) = \frac{V_{o2}}{R_2}$$

$$V_b = \frac{V_{o2}}{R_2 \left(\frac{1}{R_2} + \frac{1}{R_3} \right)}$$

$$\boxed{V_b = V_a}$$

$$\frac{V_{o2}}{R_2 \left(\frac{1}{R_2} + \frac{1}{R_3} \right)} \left(\frac{1}{R_1} + \frac{1}{R_3} \right) = \frac{V_{o1}}{R_2} + \frac{V_o}{R_3}$$

$$\frac{V_{o2}}{R_2} - \frac{V_{o1}}{R_2} = \frac{V_o}{R_3} \Rightarrow$$

$$\boxed{V_o = \frac{R_3}{R_2} (V_{o2} - V_{o1})} \quad \text{--- (1)}$$

(2) For Buffer circuit if $|V_1| > |V_2|$ should

the current across R_g ,

$$i = \frac{V_2 - V_1}{R_g} \quad \text{--- (2)}$$

the current flowing through the resistors

R_1, R_g, R_1

$$i = \frac{V_{o2} - V_{o1}}{R_1 + R_g + R_1} \quad \text{--- (3)}$$

Equate ② & ③

$$\frac{V_2 - V_1}{R_g} = \frac{V_{o2} - V_{o1}}{R_1 + R_g + R_1}$$

$$(R_1 + R_g + R_1) (V_2 - V_1) = R_g (V_{o2} - V_{o1})$$

$$(V_2 R_1 + V_2 R_g + V_2 R_1) - (V_1 R_1 + V_1 R_g + V_1 R_1) = R_g V_{o2} - V_{o1} R_g$$

$$V_2 (2R_1 + R_g) - V_1 (2R_1 + R_g) = V_{o2} - V_{o1}$$

$$\frac{V_2 (2R_1 + R_g) - V_1 (2R_1 + R_g)}{R_g} =$$

$$V_{O2} - V_{O1} = (V_2 - V_1) \frac{(2R + R_g)}{R_g}$$

$$V_{O2} - V_{O1} = (V_2 - V_1) \left(1 + 2 \frac{R_1}{R_g} \right) \quad \text{--- (2)}$$

$$V_o = \frac{R_3}{R_2} \left(1 + \frac{2R_1}{R_g} \right) (V_2 - V_1)$$

$$A = \frac{V_o}{V_2 - V_1} = \frac{R_3}{R_2} \left(1 + \frac{2R_1}{R_g} \right) \quad \text{gain}$$

If $R_1 = R_g = R$

$$A = \frac{3R_3}{R_g}$$

Advantages:

- (1) It is very stable
- (2) Accurate results
- (3) Easy to work
- (4) Reliable
- (5) scalable

Disadvantages:

- (1) During long range transmission
- (2) Noise also super imposed with the original signal

Applications:

- (1) In Bio-medical instrumentation to measure ECG
- (2) Industrial automation
- (3) used in (Pic) micro controller especially ADC

19/11/18

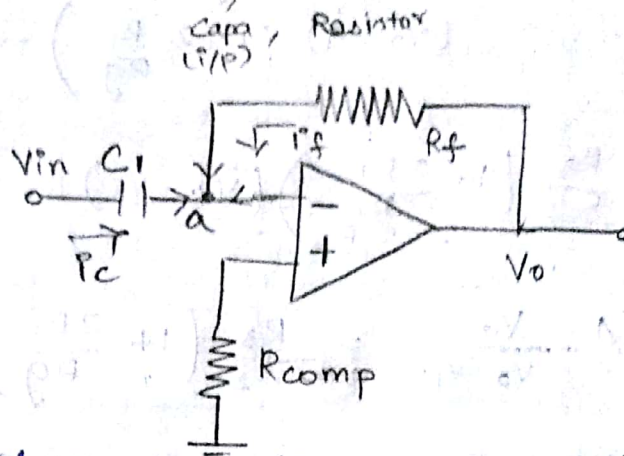
- as gate

Differentiator

other name is High pass filter

passive diff	active diff
1) RLC	1) transistor op-amp
2) no amplification	2) amplification
3) no gain	3) gain is provided

$$V_o = \frac{dv}{dt}$$



Differentiator performance = the mathematical operation (differentiation). The output voltage V_o is depend on rate of change of input voltage with respect to time. (dV/dt)

C_1 allows only ac and blocks dc (because of this differentiate of constant is 0). why it is called High pass filter?

note: impedance of capacitor = $\frac{1}{j\omega C}$

when $\omega = 0$

$$X_C \rightarrow \infty$$

so low freq signal is not allow

when $\omega = \infty$ gives a high value

then, X_C are large

$$\omega = \infty \quad X_C = 0$$

impedance $\downarrow \downarrow$ so it allow high freq signal

because of this Differentiator is known as High pass filter.

Analysis:

$$Q = C V_{in}$$

Diff. w.r. to time (or) t

$$\text{current} \rightarrow \frac{dQ}{dt} = C \cdot \frac{dV_{in}}{dt}$$

$$I = C_1 \frac{dV_{in}}{dt}$$

current across the capacitor — ①

$$\omega = 0$$

$$X_C = \infty$$

$\downarrow$
low freq
not allowed

$$\omega = \infty$$

$$X_C = 0$$

$\downarrow$
high freq
allowed

Apply KCL at node a.

$$i_c + i_f = 0 \quad (3)$$

$$i_f = \frac{V_o}{R_f} \quad (2)$$

sub (2) in (3)

$$C_1 \frac{dV_{in}}{dt} + \frac{V_o}{R_f} = 0$$

$$V_o = -R_f C_1 \frac{dV_{in}}{dt}$$

output voltage of ideal differentiator

$-R_f C_1 \rightarrow$ gain parameter

output voltage (V_o)

$R_f C_1$ times the derivative of input.

Apply Laplace transform;

Time domain $\rightarrow$ s domain

take for (H)
LT

$$V_o(s) = -R_f C_1 \cdot s V_{in}(s)$$

$$A = \frac{V_o(s)}{V_{in}(s)} = [-R_f C_1 \cdot s]$$

$$s \rightarrow j2\pi f$$

$$A = -R_f C_1 j2\pi f$$

$$f_a = \frac{1}{2\pi R_f C_1}$$

$$A = -\frac{f}{f_a}$$

$$|A| = f/f_a$$

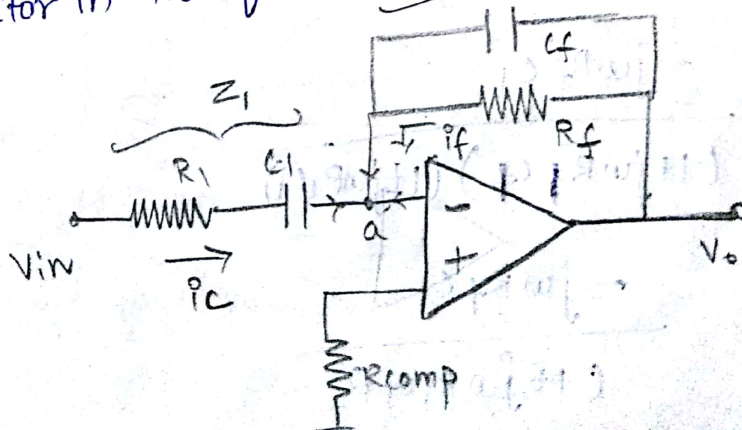
LIMITATIONS Gain vs frequency $\Rightarrow$ Inference

FOR Ideal Differentiator: the gain increases beyond

- * As frequency increases the gain increases beyond the design which make circuit unstable (oscillation)
- * At high frequency input impedance is very low which increases high frequency noise.

Practical Differentiator:

insert one Resistor R_1 at the input and capacitor in the feedback.



$$A = \frac{-Z_f}{Z_i} \quad \text{--- (*)}$$

$$Z_f = R_f \parallel \frac{1}{j\omega C_f} \quad Z_i = R_i + \frac{1}{j\omega C_i}$$

$$\frac{R_f \times \frac{1}{j\omega C_f}}{R_f + \frac{1}{j\omega C_f}} = \frac{R_f}{1 + j\omega R_f C_f} \quad \text{--- (2)}$$

$$Z_i = \frac{1 + j\omega R_i C_i}{j\omega C_i} \quad \text{--- (1)}$$

Sub (1) & (2) in (*)

$$A = \frac{-R_f}{1 + j\omega R_f C_f} \times \frac{j\omega C_i}{1 + j\omega R_i C_i}$$

$$= \frac{-j\omega R_f C_i}{(1 + j\omega R_f C_f)(1 + j\omega R_i C_i)}$$

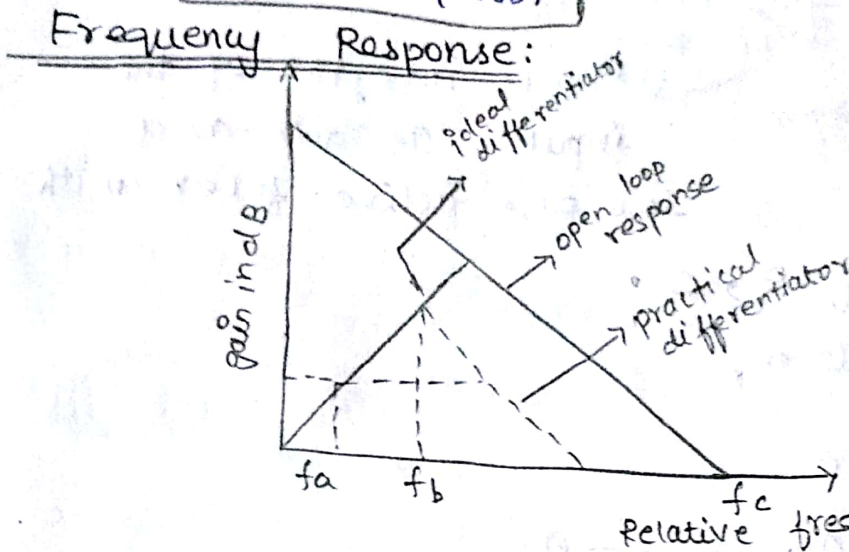
$$= \frac{-j\omega R_f C_i}{(1 + j\omega R_i C_i)(1 + j\omega R_i C_i)}$$

$$= \frac{-j\omega R_f C_i}{(1 + j\omega R_i C_i)^2}$$

$$A = \frac{-j \cdot f/f_a}{(1 + jf/f_b)^2}$$

$$|a+ib| = \sqrt{a^2+b^2}$$

$$|A| = \frac{f/f_a}{1 + (f/f_b)^2}$$



(1) open loop response oscillator has high freq of ideal diffe enter into OLR it become unstable.

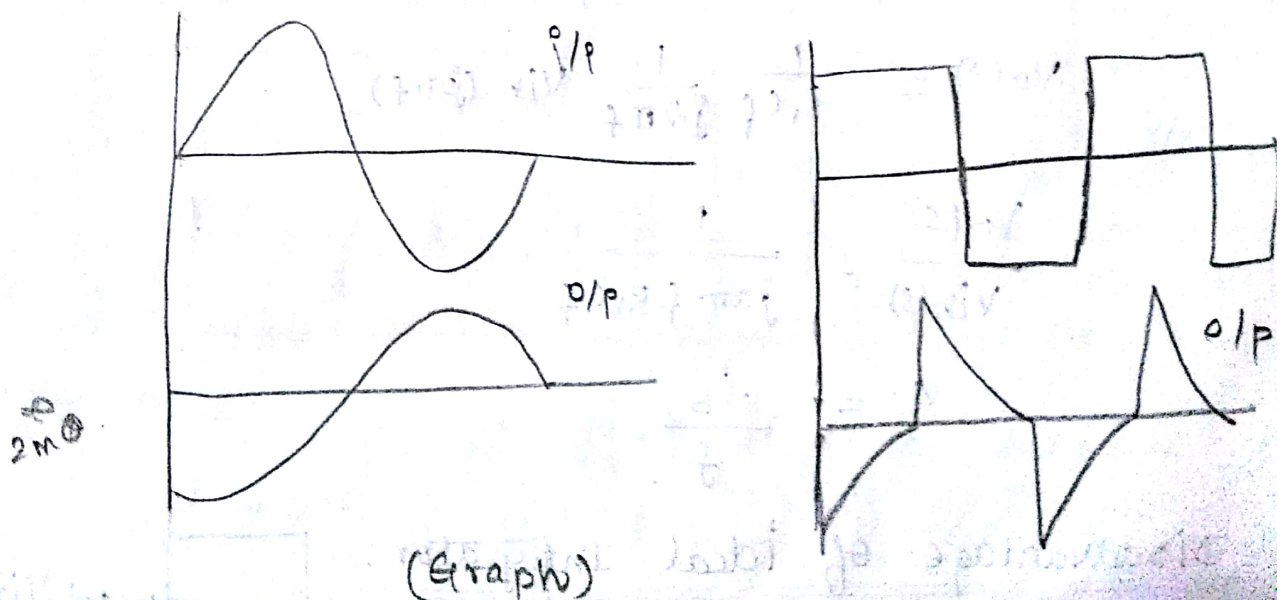
* Ideal differentiator enter into the open loop state as frequency increases.

* In a practical differentiator f_b is included after which the gain decreases by -20dB per decay.

$f_c \rightarrow$ unity gain bandwidth.

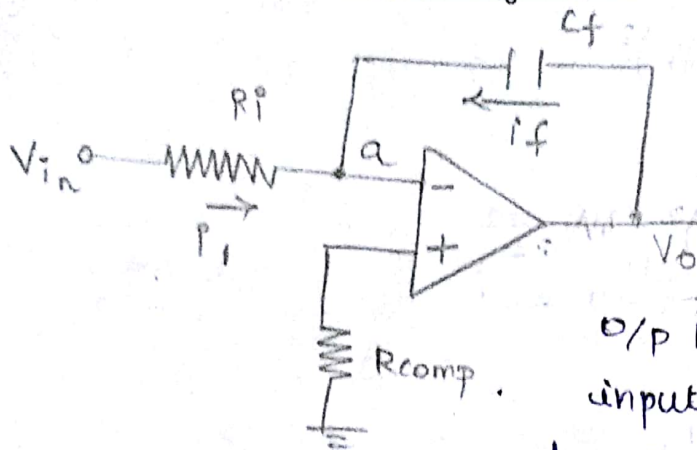
Note: For a good differentiator the time period T should be greater than or equal to $R_f C_i$.

$$T \geq R_f C_i$$



Integrator

(low pass filter)



O/p is integral of the input. It acts as a low pass active filter with

large values of R, C .

Apply KCL @ node a,

$$I_i + I_f = 0$$

$$\frac{V_{in}}{R_i} + C_f \frac{dV_o}{dt} = 0 \quad \text{--- (1)}$$

$$\frac{dV_o}{dt} = -\frac{1}{R_i C_f} V_{in} \quad \text{--- (2)}$$

integrate equ (2) on both sides,

$$V_o = -\frac{1}{R_i C_f} \int V_{in} dt \quad \text{--- (3)}$$

take LT,

$$V_o(s) = -\frac{1}{R_i C_f} \frac{1}{s} V_{in}(s) \quad f_b = \frac{1}{2\pi R_i C_f}$$

$$V_o(s) = -\frac{1}{R_i C_f} \frac{1}{j2\pi f} V_{in}(s)$$

$$\frac{V_o(s)}{V_{in}(s)} = \frac{1}{j2\pi f R_i C_f}$$

$$A = \frac{f_b}{f}$$

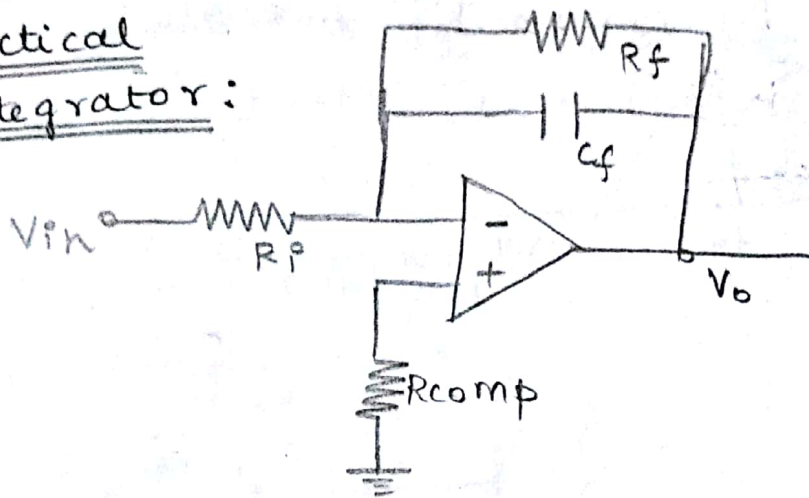
Disadvantage of Ideal Integrator:

Integrator does not have any instability problem but at low frequency, the capacitances

is zero.

Hence the gain become infinite, that is output saturate $\pm V_{sat}$. Hence we go for practical Integrator by inserting one Resistance R_f across C_f .

Practical Integrator:



Analysis,

$$Z_f = R_f \parallel C_f = R_f \parallel \frac{1}{j\omega C_f}$$

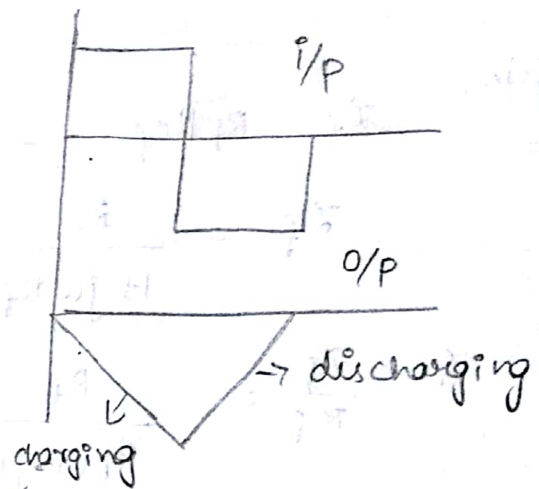
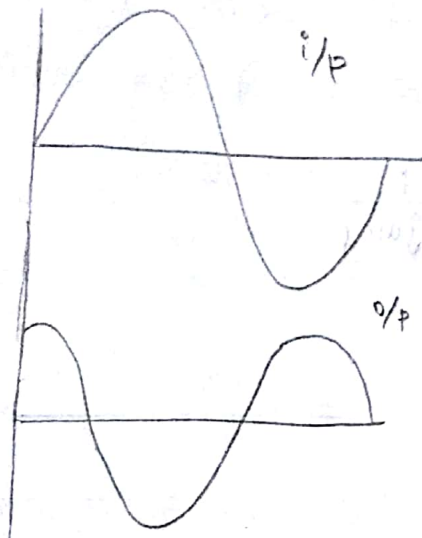
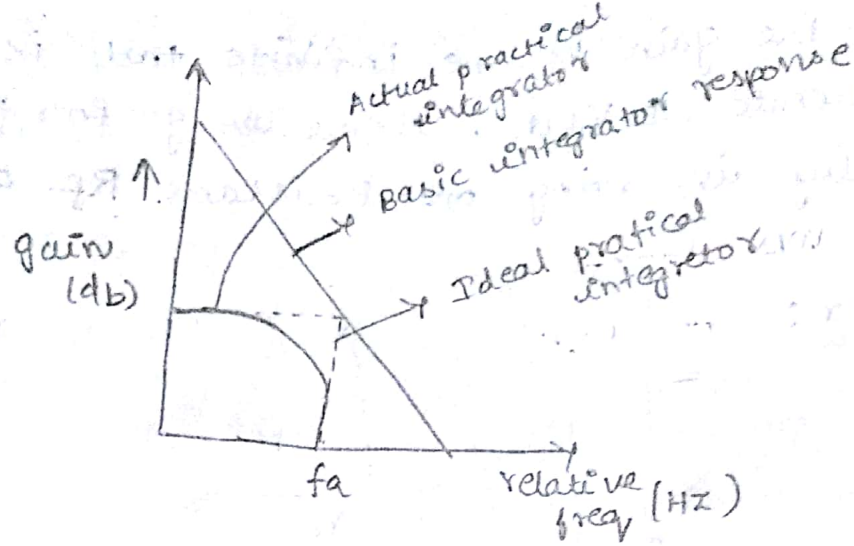
$$Z_f = \frac{R_f}{1 + j\omega R_f C_f}$$

$$A = \frac{Z_f}{R_i} = \frac{R_f}{R_i (1 + j\omega R_f C_f)}$$

$$= \frac{R_f}{R_i (1 + j2\pi f R_f C_f)}$$

$$A = \frac{R_f}{R_i (1 + jf/f_a)} \quad f_a = \frac{1}{2\pi R_f C_f}$$

$$|A| = \frac{R_f/R_i}{\sqrt{1 + (f/f_a)^2}}$$



for proper operation, (i) $R_F = 10 R_i$ (ii) $f_a = \frac{f_b}{10}$

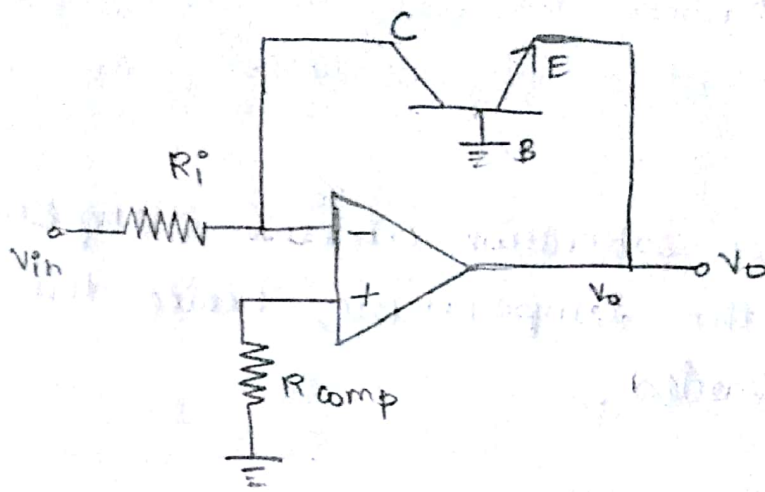
(iii) $T \gg R_f C_f$

(iv) If $f_{req} < f_a$, the integrator will act as an inverting amplifier alone and not as an integrator

shifting angle, $\theta = \tan^{-1} \left(\frac{1}{\omega R C} \right)$

Log Amplifier:

Logarithmic amplifier calculates log of i/p signal. It is used in several applications to compress dynamic range of signal. It is designed by adding and placing a diode or transistor in the feedback.



Diode current equation,

$$I_E = I_0 \left(e^{V_E / \eta V_T} - 1 \right)$$

I_0 → reverse saturation current,

V_E → V_{TE} across emitter and base

$$\frac{I_E}{I_0} = e^{V_E / \eta V_T} - 1$$

$$\ln \left(\frac{I_E}{I_0} \right) = \frac{V_E}{\eta V_T} - 1$$

$$V_E = \eta V_T \left(\ln \left(\frac{I_E}{I_0} \right) + 1 \right)$$

$$\boxed{V_E \approx \eta V_T \ln \left(\frac{I_E}{I_0} \right)}$$

$$V_E \approx \frac{KT}{q} \ln \left(\frac{I_E}{I_0} \right) \quad \left(\eta = 1 ; V_T = \frac{KT}{q} \right)$$

$$\underline{I_E \approx I_C} \quad \underline{V_E = -V_o}$$

$$V_o = - \frac{KT}{q} \ln \left(\frac{I_C}{I_0} \right)$$

to get log value
divide by 2.303

$$V_o = - \frac{KT}{q} \ln \left(\frac{V_i}{R_i I_0} \right)$$

$$I_C = \frac{V_i}{R_i}$$

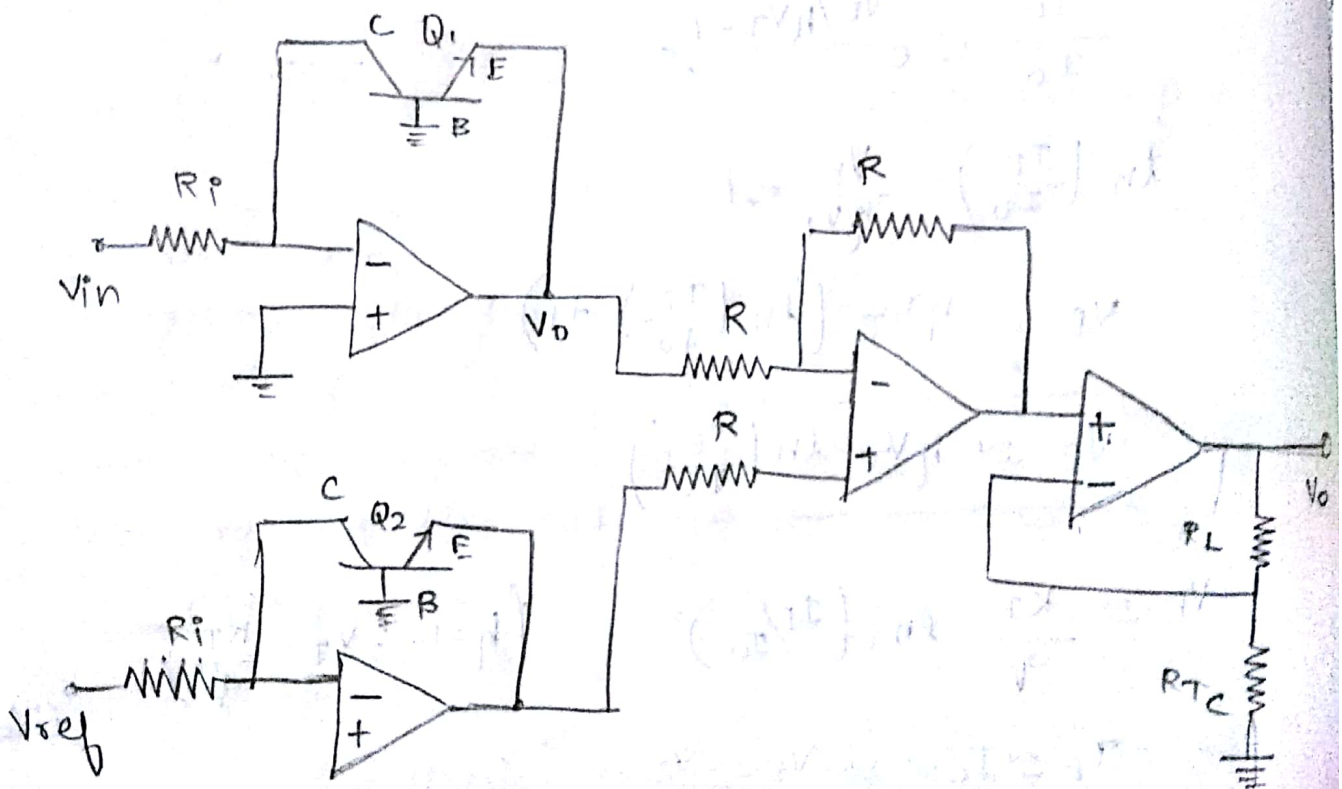
$$V_{ref} = I_0 R_i$$

Drawback:

The emitter saturation current changes with respect to the temperature, hence the o/p may be varied.

Solution for this drawback:

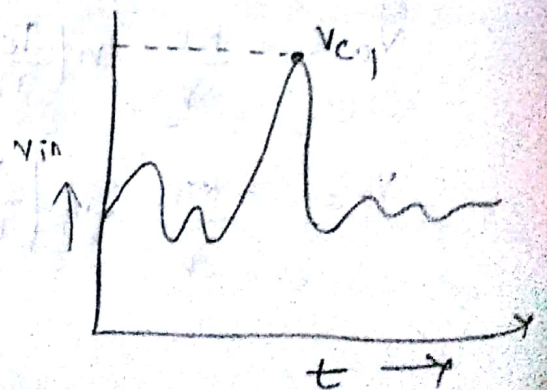
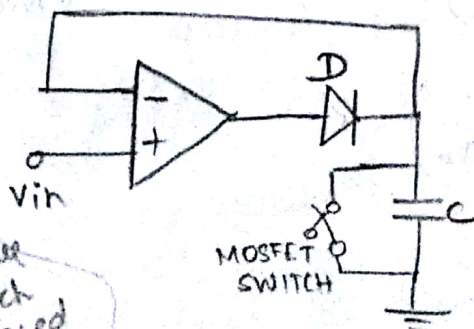
Using one thermal controlled resistor can avoid the leakage current problem due to the temperature.



Peak detector:

Diode gives the value
Switch holds the capacitor value

Changes to the peak value the switch closed



23/11/16

The inputs V_{in} or V_{ref} are given to individual log amplifier and output are given to the differential amplifier.

stage 1 - log amplifier

stage 2 - differential amplifier

stage 3 - non inverting amplifier

from (V_o)

$$V_1 = \frac{-KT}{q} \ln \left(\frac{V_i}{I_o R_i} \right) \quad V_2 = \frac{-KT}{q} \ln \left(\frac{V_{ref}}{I_o R_i} \right)$$

$$V_o' = V_2 - V_1 \text{ (Differential amplifier)}$$

$$= \frac{-KT}{q} \ln \left(\frac{V_{ref}}{I_o R_i} \right) - \left(\frac{-KT}{q} \ln \left(\frac{V_i}{I_o R_i} \right) \right)$$

$$= \frac{KT}{q} \left[-\ln \left(\frac{V_{ref}}{I_o R_i} \right) - \left(-\ln \left(\frac{V_i}{I_o R_i} \right) \right) \right]$$

$$= \frac{KT}{q} \ln \left[\frac{V_{ref}}{I_o R_i} \right] \times \left[\frac{I_o R_i}{V_i} \right]$$

$$\begin{aligned} \log a + \log b &= \log a \log b \\ &= \frac{\log b}{\log a} \end{aligned}$$

$$V_o' = \frac{KT}{q} \ln \frac{V_{ref}}{V_i}$$

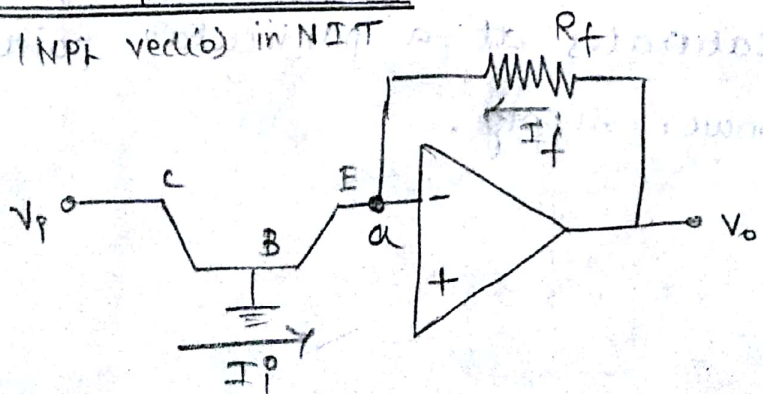
non-inverting amplifier:

$$V_o = \left(1 + \frac{R_2}{R_{TC}} \right) V_o'$$

$$= \left(1 + \frac{R_2}{R_{TC}} \right) \left(\frac{KT}{q} \ln \frac{V_{ref}}{V_i} \right)$$

ANTI LOG AMPLIFIER:

(NPT vedio) in NIT



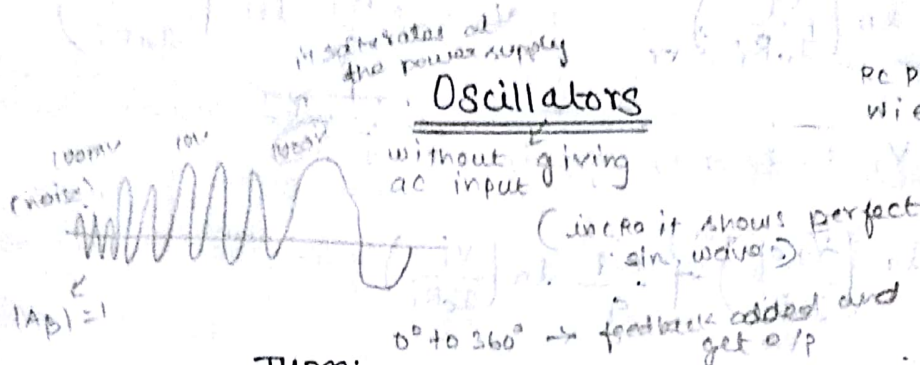
$$I_i + I_f = 0$$

$$I_o e^{\frac{V_i}{R_T}} + \frac{V_o}{R_f} = 0$$

$e^x \rightarrow \text{antilog}$

$$V_o = -R_f I_o e^{V_i/R_T}$$

$$V_o = -R_f I_o e^{V_i/R_T}$$



pc phase shift
Wien bridge → not having phase shift

Hartley Colpitts

Types:

- (i) RC phase shift (ii) Wien bridge
(audio frequency)

local oscillator → to generate carrier signal

crystal oscillator → used in watch very important

to produce sound

oscillator

* It produces AC output without any AC input. The source for output signal is the noise voltage provided by the transistor mismatch (leakage current).

* oscillator has +ve feedback.

* In necessary condition for oscillation

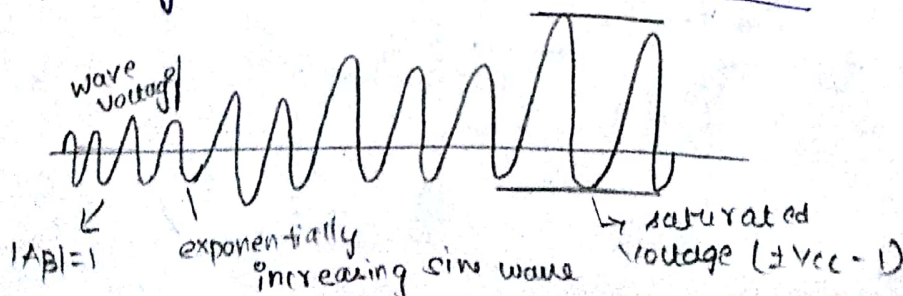
is

(i) $|A\beta| = 1$

(ii) total phase shift is 0° or 360°

Note:

oscillator produce sine wave (exponentially growing sine wave) and it saturates at a particular point decided by the power supply.

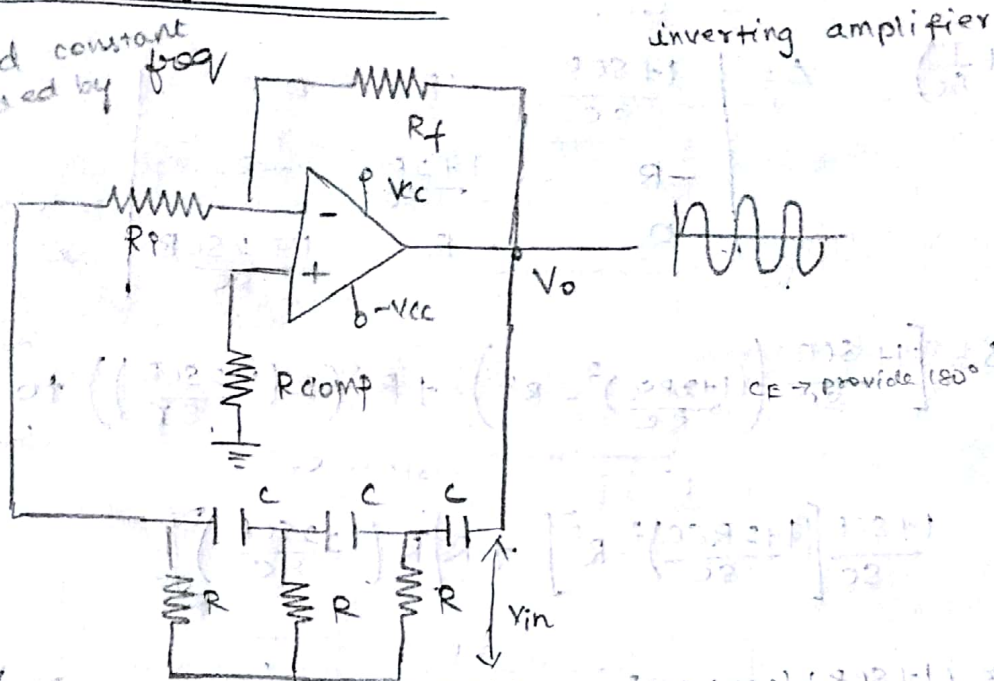


Types of Oscillator:

- (i) RC phase shift
 - (ii) Wien bridge
- } → Audio frequency oscillator
upto 20 KHz

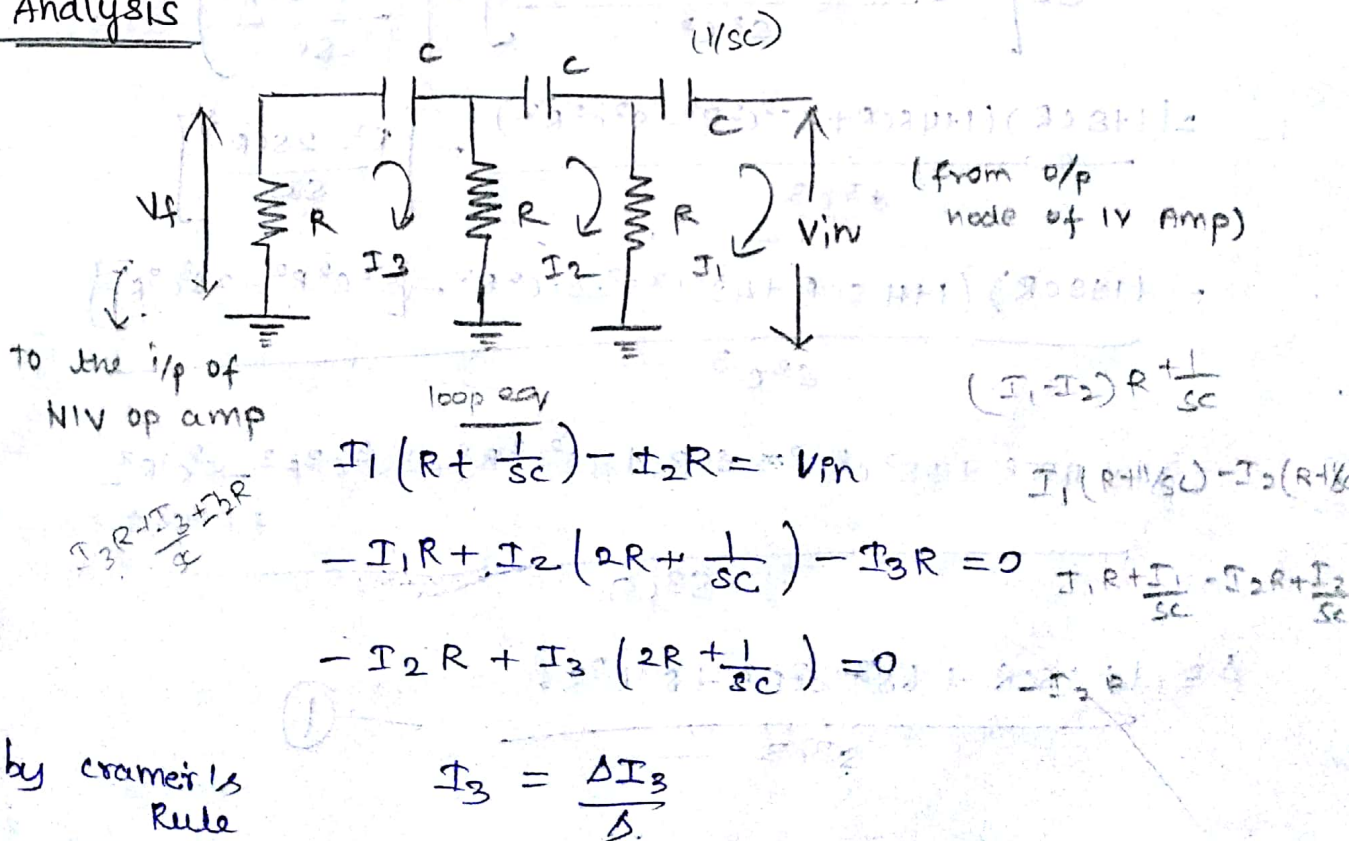
RC phase shift oscillator:

Time period constant
it is decided by f_{osc}



It has an inverting amplifier which provides 180° phase shift. Feedback network with 3 RC component provide another 180° (1 RC pair provide 60° phase shift). $\theta = \tan^{-1} \frac{1}{\omega RC}$.

Analysis



$$\Delta = \begin{vmatrix} R_1 + \frac{1}{sC} & -R & 0 \\ -R & 2R + \frac{1}{sC} & -R \\ 0 & -R & 2R + \frac{1}{sC} \end{vmatrix} \begin{vmatrix} I_1 \\ I_2 \\ I_3 \end{vmatrix} = \begin{vmatrix} V_{in} \\ 0 \\ 0 \end{vmatrix}$$

$$(R_1 + \frac{1}{sC}) \Delta = \begin{vmatrix} \frac{1+sCR}{sC} & -R & 0 \\ -R & \frac{1+2RSC}{sC} & -R \\ 0 & -R & \frac{1+2SCR}{sC} \end{vmatrix}$$

$$\Delta = \left[\frac{1+sCR}{sC} \left(\left(\frac{1+2RSC}{sC} \right)^2 - R^2 \right) + R \left(R \left(\frac{1+2SCR}{sC} \right) \right) + 0 \right]$$

$$\Delta = \frac{1+sCR}{sC} \left[\left(\frac{1+2RSC}{sC} \right)^2 - R^2 \right] + R \left[R \left(\frac{1+2SCR}{sC} \right) \right]$$

$$\Delta = \left(\frac{1+sCR}{sC} \right) \left(\frac{1+2RSC}{sC} \right)^2 - R^2 \left(\frac{1+sCR}{sC} \right) + R \left[R \left(\frac{1+2SCR}{sC} \right) \right]$$

$$\Delta = \frac{1+sCR}{sC} \left[\left(\frac{1+2RSC}{sC} \right)^2 - R^2 \right] + R \left[R \left(\frac{1+2SCR}{sC} \right) \right]$$

$$\Delta = \frac{1+sCR}{sC} \left[\frac{1+4sCR+4s^2C^2R^2-s^2C^2R^2}{s^2C^2} \right] - \left[\frac{R^2-2sCR^3}{sC} \right]$$

$$= \frac{(1+sCR)(1+4sCR+4s^2C^2R^2-s^2C^2R^2)}{s^3C^3} - \left[\frac{R^2-2sCR^3}{sC} \right]$$

$$= \frac{(1+sCR)(1+4sCR+4s^2C^2R^2-s^2C^2R^2) - [s^2C^2R^2-2s^3C^3R^3]}{s^3C^3}$$

$$= \frac{1+4sCR+3s^2C^2R^2+sCR+4s^2C^2R^2+3s^3C^3R^3-s^2C^2R^2-2s^3C^3R^3}{s^3C^3}$$

$$\Delta = \frac{1+5sCR+6s^2C^2R^2+s^3C^3R^3}{s^3C^3}$$

①

$$\Delta_3 = \begin{vmatrix} \frac{1+5RC}{sC} & -R & V_{in} \\ -R & \frac{1+2sRC}{sC} & 0 \\ 0 & -R & 0 \end{vmatrix} = V_{in}(R^2) \quad (2)$$

sub (1) & (2)

$$I_3 = \frac{\Delta_3}{\Delta}$$

$$I_3 = \frac{1+5sRC+6s^2C^2R^2+s^3C^3R^3}{s^3C^3} \times V_{in}R^2$$

$$I_3 = \frac{V_{in}R^2s^3C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3} \quad (3)$$

$$V_f = I_3 R$$

$$V_f = \frac{V_{in}s^3C^3R^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3}$$

$$\frac{V_f}{V_{in}} = \frac{s^3C^3R^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3}$$

$$\beta = \frac{1}{\frac{1}{s^3C^3R^3} + \frac{5}{s^2C^2R^2} + \frac{6}{sCR} + 1}$$

$$s \rightarrow j\omega \quad s^2 = -\omega^2 \quad s^3 = -j\omega^3$$

$$\beta = \frac{1}{\frac{1}{-j\omega^3C^3R^3} + \frac{5}{(-\omega^2C^2R^2)} + \frac{6}{j\omega CR} + 1}$$

img

$$\beta = \frac{1}{-j\omega^3C^3R^3 - \frac{5}{\omega^2C^2R^2} + \frac{6}{j\omega CR} + 1}$$

no
there is no
angle hence

since phase shift is '0' $\text{Im}g \text{ part} = 0$

$$\frac{b}{\omega CR} - \frac{1}{\omega^3 C^3 R^3} = 0$$

$$\frac{b}{\omega CR} = \frac{1}{\omega^3 C^3 R^3}$$

$$b = \frac{1}{\omega^2 C^2 R^2} \quad (4)$$

$$\omega^2 = \frac{1}{b C^2 R^2}$$

$$\beta = \frac{1}{1 - \frac{5}{\omega^2 C^2 R^2}}$$

$$\omega = \frac{1}{\sqrt{b} CR}$$

$$2\pi f = \frac{1}{RC \sqrt{b}}$$

$$f = \frac{1}{2\pi RC \sqrt{b}}$$

$$|A\beta| = 1$$

$$A = 1/\beta$$

$$A = 1 - \frac{5}{\omega^2 C^2 R^2}$$

from (4)

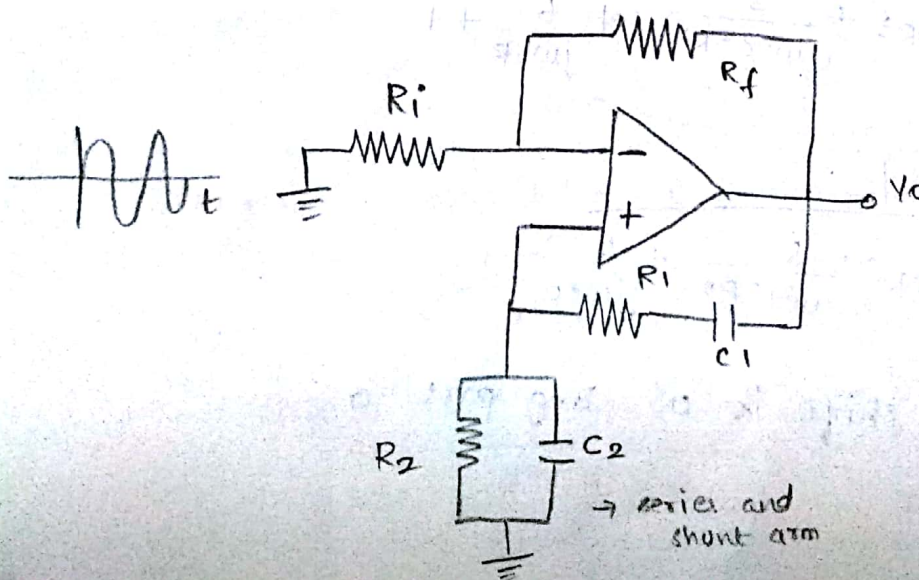
$$A = 1 - 5(6) = 1 - 30 = -29$$

$$|A| \geq 29$$

Necessary value of gain for RC phase shift oscillator.

25/11/18

WIEN BRIDGE OSCILLATOR



(1) non-inverting amplifier

(2) It P

(3)

used for impedance matching

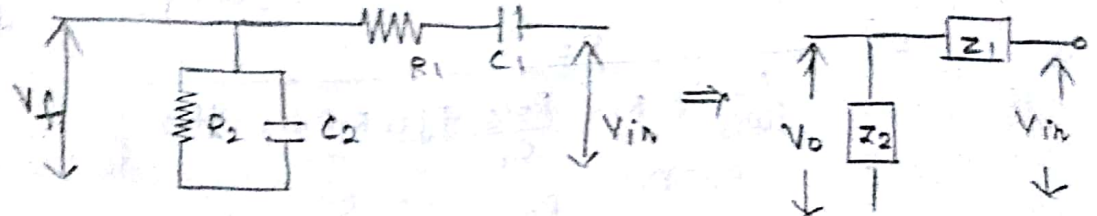
If no series & shunt arm

→ series and shunt arm

Wien bridge oscillator has 2 stages

- (1) non-inverting amplifier
- (2) Feedback stage which consists of series and shunt arm.

Total phase shift around the loop is 0° . The Bridges use to produce sustain oscillation under balanced condition.



$$Z_1 = R_1 + \frac{1}{sC_1}$$

$$Z_2 = R_2 \parallel \frac{1}{sC_2}$$

$$Z_1 = \frac{R_1 sC_1 + 1}{sC_1} \Rightarrow \boxed{\frac{1 + R_1 sC_1}{sC_1}}$$

$$Z_2 = \frac{(R_2) \left(\frac{1}{sC_2}\right)}{R_2 + \frac{1}{sC_2}} = \frac{R_2 \left(\frac{1}{sC_2}\right)}{\frac{R_2 sC_2 + 1}{sC_2}}$$

by voltage divider rule,

$$Z_2 = \frac{R_2}{R_2 sC_2 + 1} \quad (\text{or}) \quad \boxed{\frac{R_2}{1 + R_2 sC_2}}$$

$$V_f = V_{in} \frac{Z_2}{Z_1 + Z_2}$$

$$\beta = \frac{V_f}{V_{in}} = \frac{Z_2}{Z_1 + Z_2}$$

$$\beta = \frac{R_2}{1 + R_2 sC_2}$$

$$\left[\frac{1 + sR_1C_1}{sC_1} \right] + \left[\frac{R_2}{1 + sR_2C_2} \right]$$

$$\beta = \frac{\frac{R_2}{1 + sR_2C_2}}{\left[\frac{1 + sR_1C_1}{sC_1} \right] + \left[\frac{R_2}{1 + sR_2C_2} \right]}$$

$$= \frac{R_2}{(1 + sR_1C_1)(1 + sR_2C_2) + R_2(sC_1)}$$

$$= \frac{sR_2C_1}{(1 + sR_1C_1)(1 + sR_2C_2) + sR_2C_1}$$

$s \rightarrow j\omega$

$$= \frac{j\omega R_2 C_1}{(1+j\omega R_1 C_1)(1+j\omega R_2 C_2) + j\omega R_2 C_1}$$

$$= \frac{j\omega R_2 C_1}{1+j\omega R_2 C_2 + j\omega R_1 R_2 - \omega^2 R_1 R_2 C_1 C_2 + j\omega R_2 C_1}$$

$$\beta = \frac{R_2}{\frac{1}{j\omega C_1} + \frac{j\omega R_1 C_1}{j\omega C_1} + \frac{j\omega R_2 C_2}{j\omega C_1} - \frac{\omega^2 R_1 R_2 C_1 C_2}{j\omega C_1} + \frac{j\omega R_2 C_1}{j\omega C_1}}$$

$$= \frac{R_2}{\frac{1}{j\omega C_1} + R_1 + \frac{R_2 C_2}{C_1} + j\omega R_1 R_2 C_2 + R_2}$$

$$= \frac{R_2}{R_1 + R_2 + \frac{R_2 C_2}{C_1} + j\omega R_1 R_2 C_2 - \frac{j}{\omega C_1}}$$

$$= \frac{R_2}{\frac{R_1 C_1 + R_2 C_1 + R_2 C_2}{C_1} + \frac{(1 - \omega^2 R_1 R_2 C_1 C_2)}{j\omega C_1}}$$

Imaginary part = 0

$$-\frac{1 - \omega^2 R_1 R_2 C_1 C_2}{\omega C_1} = 0$$

$$1 - \omega^2 R_1 R_2 C_1 C_2 = 0$$

$$1 = \omega^2 R_1 R_2 C_1 C_2$$

$$\omega^2 = \frac{1}{R_1 R_2 C_1 C_2}$$

$$\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$2\pi f = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$f = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}}$$

real part

$$P = \frac{R_2 C_1}{R_1 C_1 + R_2 C_2 + R_2 C_1}$$

$$|A\beta| = 1$$

$$|A| = \frac{1}{|\beta|}$$

$$|A| = \frac{R_1 C_1 + R_2 C_2 + R_2 C_1}{R_2 C_1}$$

If we assume $R_1 = R_2 = R$ (with variable resistance)

$$C_1 = C_2 = C$$

$$f = \frac{1}{2\pi \sqrt{R_1 C_1 C_2 R_2}} = \frac{1}{2\pi \sqrt{R^2 C^2}}$$

$$f = \frac{1}{2\pi RC}$$

NOTE:

(1) To prevent loading effect R_1 is selected such that R_1 is $R_1 \leq 10R_2$ in RC phase shift oscillator.

$$|A| = \frac{RC + RC + RC}{RC} = \frac{3RC}{RC}$$

$$|A| = 3$$

The minimum gain require to sustain oscillator is

$$A = 3$$

D Design a phase shift oscillator to oscillate at 100Hz
assume $C = 0.1 \mu F$.

$$C = 0.1 \mu$$

$$f = 100 \text{ Hz}$$

$$R = ?$$

For RC phase shift:

$$f = \frac{1}{2\pi RC \sqrt{6}}$$

$$100 \text{ Hz} = \frac{1}{2\pi R (0.1 \mu) \sqrt{6}}$$

$$R = \frac{1}{2\pi \times 100 \times 0.1 \mu \sqrt{6}} = 6.49 \text{ K}\Omega$$

$$R_1 = 10 \times R = 64 \text{ K}\Omega$$

$$|A| > 29$$

$$|A| = 29 \text{ (phase shift } R_c)$$

$$|A| = -\frac{R_f}{R_i}$$

$$\text{Inverting } \Rightarrow (-29) = -\frac{R_f}{64K}$$

$$\therefore -29 \times 64K = -R_f$$

$$R_f = 1.84MK$$

For Wien bridge:

$$f = \frac{1}{2\pi RC} \Rightarrow R = \frac{1}{2\pi \times 100 \times 0.1\mu F} = 16K\Omega$$

$$R_i = 10 \times R = 10 \times 16 = 160K\Omega$$

$$|A| = 3$$

$$|A| = 1 + \frac{R_f}{R_i}$$

$$3 = 1 + \frac{R_f}{160K}$$

$$3 = \frac{160K + R_f}{160K} \Rightarrow 160K \times 3 = 160K + R_f$$

$$480K - 160K = R_f$$

$$R_f = 320K\Omega$$

FILTERS:

Types of filters:

① LPF (Low pass filter) →



② HPF (High pass filter) →

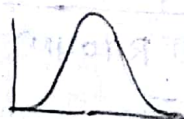


③ BPF (Bandpass filter)

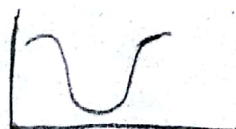


WBPF
(wideband pass)

NBPF
(narrow bandpass)



④ BRF (Band Reject filter)

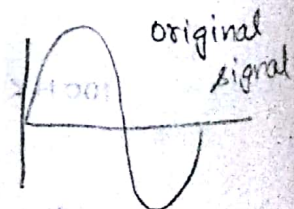


Analog filter

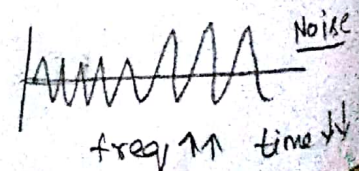
RLC Transistor

Digital filter

Registers



frequency time period



frequency time

Active filter:

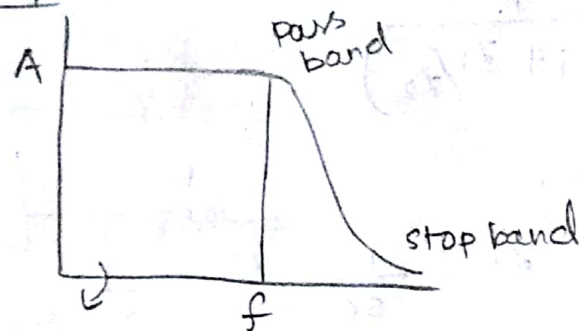
Do 2 tasks

- (i) Amplification (ii) filtering

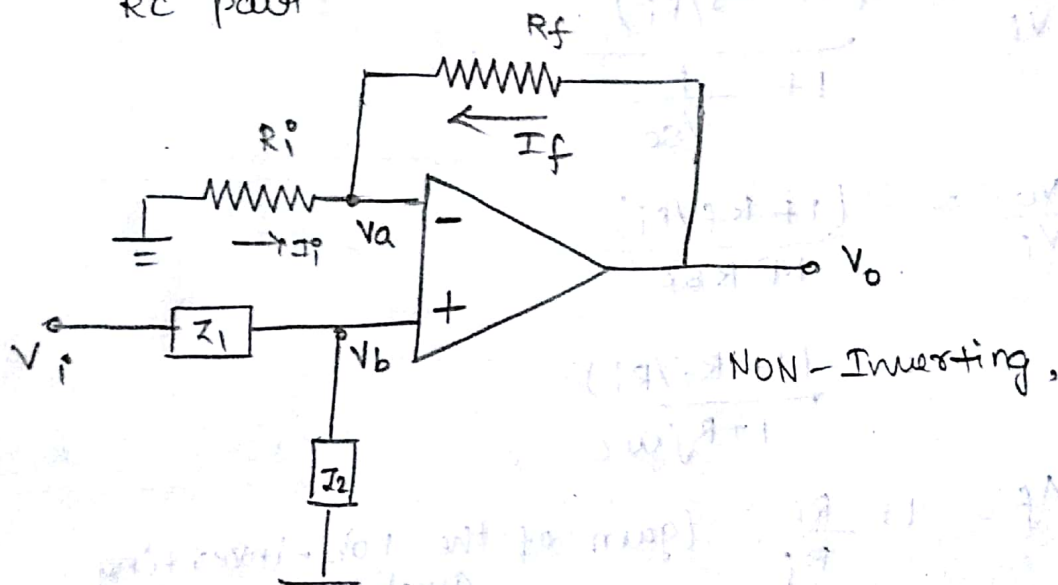
These LPF, HPF, BPF, BRF are used in demodulation.

① LOW PASS FILTER:

model graph:



order is dependent on RC pair



NON-Inverting,

Apply node equation,

apply node a,

$$\frac{V_a}{R_i} + \frac{V_a - V_o}{R_f} = 0$$

$$V_a = \frac{V_o}{R_f \left(\frac{1}{R_i} + \frac{1}{R_f} \right)}$$

apply node b,

$$\frac{V_b - V_i}{Z_1} + \frac{V_b}{Z_2} = 0$$

$$V_b = \frac{V_i}{Z_1 \left[\frac{1}{Z_1} + \frac{1}{Z_2} \right]}$$

By virtual gnd, $V_a = V_b$

$$\frac{V_i}{z_1 \left[\frac{1}{z_1} + \frac{1}{z_2} \right]} = \frac{V_o}{R_f \left(\frac{1}{R_i} + \frac{1}{R_f} \right)}$$

$$\frac{V_o}{V_i} = \frac{R_f \left(\frac{1}{R_i} + \frac{1}{R_f} \right)}{z_1 \left[\frac{1}{z_1} + \frac{1}{z_2} \right]}$$

$$\frac{V_o}{V_i} = \frac{\left(1 + \frac{R_f}{R_i} \right)}{\left(1 + \frac{z_1}{z_2} \right)}$$

for low pass filter,

put $z_1 = R$ $z_2 = \frac{1}{sC}$

$$\frac{V_o}{V_i} = \frac{\left(1 + \frac{R_f}{R_i} \right)}{1 + \frac{R}{1/sC}}$$

$$\frac{V_o}{V_i} = \frac{\left(1 + \frac{R_f}{R_i} \right)}{1 + R s C}$$

$$= \frac{\left(1 + \frac{R_f}{R_i} \right)}{1 + R j \omega C}$$

$A_f = 1 + \frac{R_f}{R_i}$ (gain of the non-inverting amplifier)

$A = \frac{V_o}{V_i}$ (gain of filter)

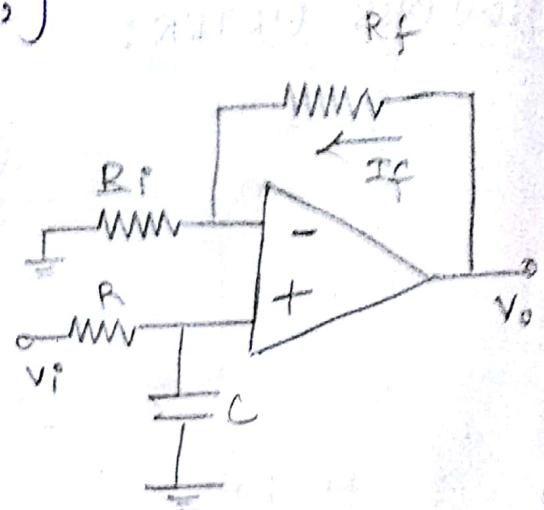
$$f_L = \frac{1}{2\pi R C}$$

$$A = \frac{A_f}{1 + j 2\pi f R C}$$

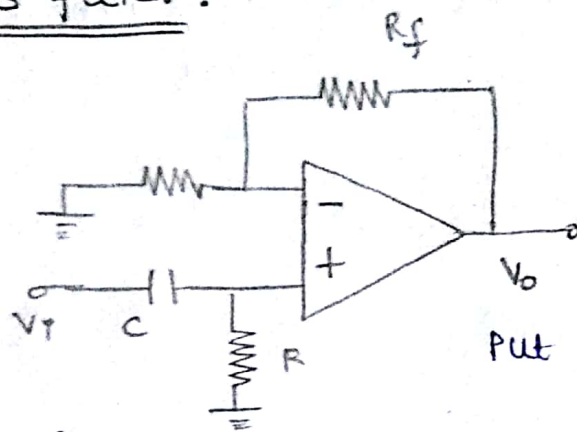
$$A = \frac{A_f}{1 + j f / f_L}$$

gain of low pass filter

$$|A| = \frac{A_f}{\sqrt{1 + (f/f_L)^2}}$$



② High pass filter :



Put $Z_1 = 1/sC$; $Z_2 = R$

$$A = \frac{A_f}{1 + \frac{1/sC}{R}}$$

$$A = \frac{A_f}{1 + \frac{1}{sCR}}$$

$$A = \frac{A_f}{1 + \frac{1}{j2\pi fRC}}$$

$$f_H = \frac{1}{2\pi RC}$$

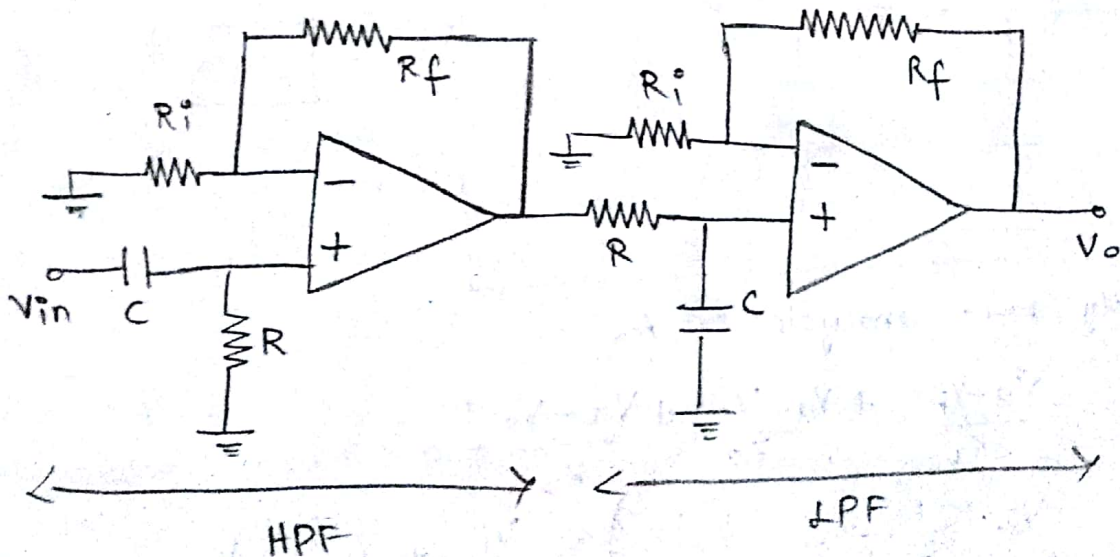
$$A = \frac{A_f}{1 + jf_H/f}$$

$$|A| = \frac{A_f}{\sqrt{1 + (f_H/f)^2}}$$

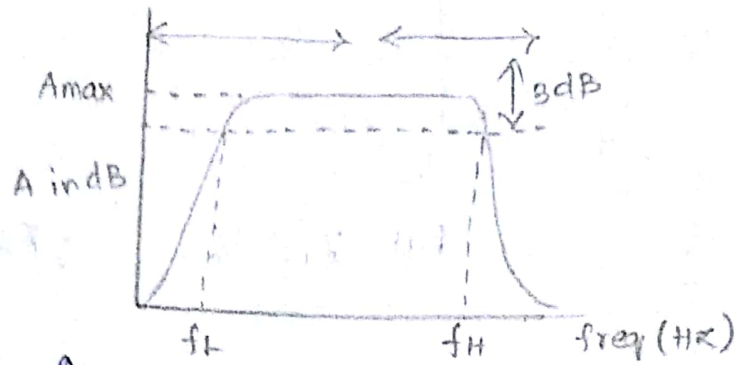
③ Band pass filter :

$$A_{BPF} = A_H \times A_L$$

$$A_{BPF} = \frac{A_f^2}{\sqrt{1 + (f/f_L)^2} \sqrt{1 + (f_H/f)^2}}$$



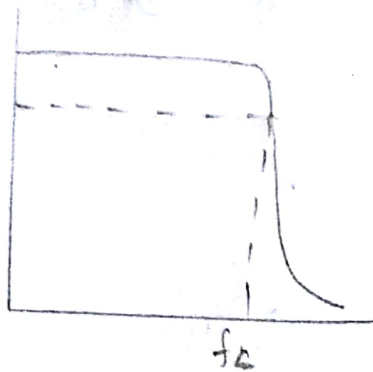
Band Pass Filter



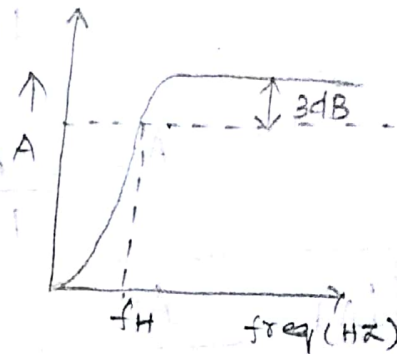
$$A_L = \frac{A_f}{\sqrt{1 + (f/f_L)^2}}$$

$$A_H = \frac{A_f}{\sqrt{1 + (f_H/f)^2}}$$

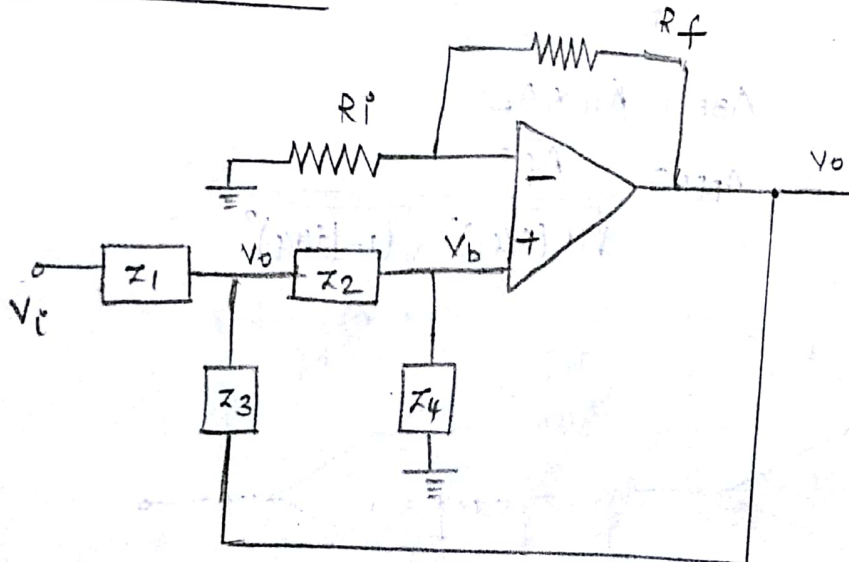
LPF



HPE



IInd order Filters:



$$\frac{1}{Z} = Y$$

Apply node analysis on A ,

$$\frac{V_a - V_b}{Z_1} + \frac{V_a - V_b}{Z_2} + \frac{V_a - V_o}{Z_3} = 0$$

$$V_a \left(\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3} \right) = \frac{V_i}{Z_1} + \frac{V_b}{Z_2} + \frac{V_o}{Z_3} \quad \text{--- ①}$$

$$V_a(Y_1 + Y_2 + Y_3) = V_i Y_1 + V_b Y_2 + V_o Y_3 \quad \text{--- (2)} \quad Y_1 = Y$$

@ node b,

$$\frac{V_i - V_a}{Z_2} + \frac{V_b}{Z_4} = 0$$

$$\frac{V_b}{Z_2} + \frac{V_b}{Z_4} = \frac{V_o}{Z_2}$$

$$V_b(Y_2 + Y_4) = V_o Y_2$$

$$V_a = \frac{V_b(Y_2 + Y_4)}{Y_2} \quad \text{--- (3)}$$

③ in ②

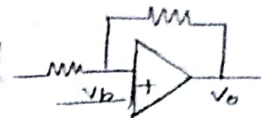
$$V_b \frac{(Y_2 + Y_4)}{Y_2} (Y_1 + Y_2 + Y_3) = V_i Y_1 + V_b Y_2 + V_o Y_3$$

$$\frac{V_b (Y_2 + Y_4) (Y_1 + Y_2 + Y_3) - V_b Y_2}{Y_2} = V_i Y_1 + V_o Y_3$$

$$V_b \left[\frac{(Y_2 + Y_4) (Y_1 + Y_2 + Y_3) - Y_2^2}{Y_2} \right] = V_i Y_1 + V_o Y_3 \quad \text{--- (4)}$$

$$A_f = \frac{V_o}{V_b}$$

$$V_b = \frac{V_o}{A_f} \quad \text{--- (5)}$$



sub in (4)

$$\frac{V_o}{A_f} \left[\frac{(Y_2 + Y_4) (Y_1 + Y_2 + Y_3) - Y_2^2}{Y_2} \right] = V_i Y_1 + V_o Y_3$$

$$\frac{V_o}{A_f Y_2} \left[(Y_2 + Y_4) (Y_1 + Y_2 + Y_3) - Y_2^2 \right] - V_o Y_3 = V_i Y_1$$

$$V_o \left[\frac{(Y_2 + Y_4) (Y_1 + Y_2 + Y_3) - Y_2^2}{A_f Y_2} - Y_3 \right] = V_i Y_1$$

$$V_o \left[\frac{(Y_2 + Y_4) (Y_1 + Y_2 + Y_3) - Y_2^2 - Y_3 A_f Y_2}{A_f Y_2} \right] = V_i Y_1$$

$$V_o \left[\frac{(Y_2 Y_1 + Y_2^2 + Y_2 Y_3 + Y_4 Y_1 + Y_4 Y_2 + Y_4 Y_3) - Y_2^2 - A_f Y_2 Y_3}{A_f Y_2} \right] = V_i Y_1$$

$$V_o \left[\frac{Y_2 Y_1 + Y_2 Y_3 + Y_4 Y_1 + Y_4 Y_2 + Y_4 Y_3 - A_f Y_2 Y_3}{A_f Y_2} \right] = V_i Y_1$$

$$V_o [Y_1 Y_2 + Y_4 (Y_1 + Y_2 + Y_3) + Y_2 Y_3 (1 - A_f)] = V_i Y_1 Y_2 A_f$$

$$A = \frac{V_o}{V_i} = \frac{Y_1 Y_2 A_f}{(Y_1 Y_2 + Y_4 (Y_1 + Y_2 + Y_3) + Y_2 Y_3 (1 - A_f))} \quad \text{--- (6)}$$

second order low pass filter

$$Y_1 = Y_2 = R$$

$$Y_3 = Y_4 = sC$$

$$Y_1 = Y_2 = \frac{1}{R}$$

$$Y_3 = Y_4 = sC$$

--- (7)

sub (7) in (6)

$$A = \frac{V_o}{V_i} = \frac{(\frac{1}{R})(\frac{1}{R}) A_f}{(\frac{1}{R})(\frac{1}{R}) + sC (\frac{1}{R} + \frac{1}{R} + sC) + (\frac{1}{R}) sC (1 - A_f)}$$

$$= \frac{\frac{1}{R^2} A_f}{\frac{1}{R^2} + sC (\frac{1}{R} + \frac{1}{R} + sC) + (\frac{1}{R} sC) (1 - A_f)}$$

$$= \frac{\frac{1}{R^2} A_f}{\frac{1}{R^2} + sC \left[\frac{2 + sCR}{R} \right] + \frac{sC}{R} [1 - A_f]}$$

$$= \frac{\cancel{\frac{1}{R^2}} A_f}{\frac{1 + sCR(2 + sCR) + sCR(1 - A_f)}{\cancel{R^2}}}$$

$$A = \frac{A_f}{1 + 2sCR + sCR^2 + sCR - A_f sCR}$$

$$A = \frac{A_f}{1 + 3sCR + sCR^2 - sCRA_f}$$

$$A = \frac{A_f}{1 + sCR(3 - A_f) + sCR^2}$$

1/21/15

$$A = \frac{A_f}{1 + sCR(3 - A_f) + s^2 R^2 C^2}$$

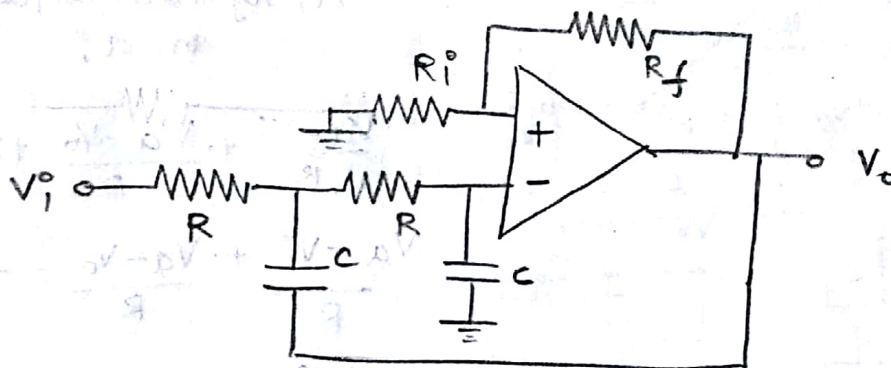
$$A = \frac{A_f}{1 + \alpha sCR + s^2 C^2 R^2}$$

$$= \frac{A_f}{1 + \alpha j^2 \pi f (CR + (j^2 \pi f)^2 C^2 R^2)}$$

$$\begin{aligned} A_f &= 3 - \alpha \\ \alpha &= 3 - A_f \end{aligned}$$

$$= \frac{A_f}{1 + \alpha j^2 f/f_L - (f/f_L)^2}$$

$$|A| = \frac{A_f}{\sqrt{(1 - (f/f_L)^2)^2 + (\alpha f/f_L)^2}}$$



2) High pass Filter :

$$Z_1 = Z_2 = 1/sC \quad Y_1 = Y_2 = sC$$

$$Z_3 = Z_4 = R \quad Y_3 = Y_4 = 1/R$$

$$|A| = \frac{A_f}{\sqrt{1 - (f/f_H)^2)^2 + (\alpha f/f_H)^2}}$$

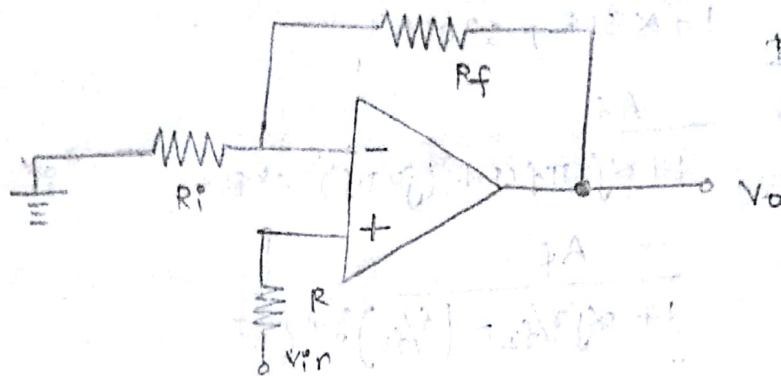
3) Band pass filter :

BPF = low pass filter gain $\times$ High pass filter gain

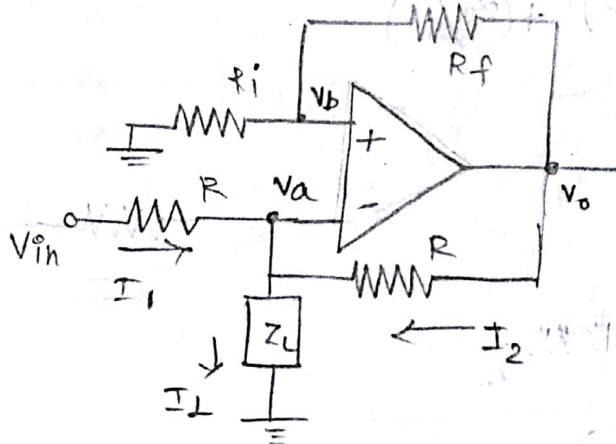
VOLTAGE TO CURRENT converter (or) V-I converter :

i_p is through resistor $\leftarrow$ J-V $\rightarrow$ C-V converter
 $NIV \rightarrow i/p$ directly given to the op-amp
 Voltage

V-I converter other name is trans conductance amplifier. A non-inverting amplifier is an voltage to current converter.



V-I using floating load.



Apply node equation on a,

$$\frac{V_a - V_i}{R} + \frac{V_a - V_o}{R} + I_L = 0$$

$$\frac{V_a - V_i}{R} + \frac{V_a - V_o}{R} = -I_L$$

$$V_a - V_i + V_a - V_o = -I_L R$$

$$2V_a = V_i + V_o - I_L R$$

$$V_a = \frac{V_i + V_o - I_L R}{2} \quad \text{--- (1)}$$

$$A = 1 + \frac{R_f}{R_i}$$

$$R_f = R_i = R$$

$$A = 1 + \frac{R}{R} = 1 + 1$$

$$\boxed{A = 2}$$

$$\frac{V_o}{V_i} = 2$$

$$V_o = 2V_i$$

Apply node equation on node b,

$$\frac{V_b}{R_i} + \frac{V_b - V_o}{R_f} = 0$$

$$R_i = R_f = R$$

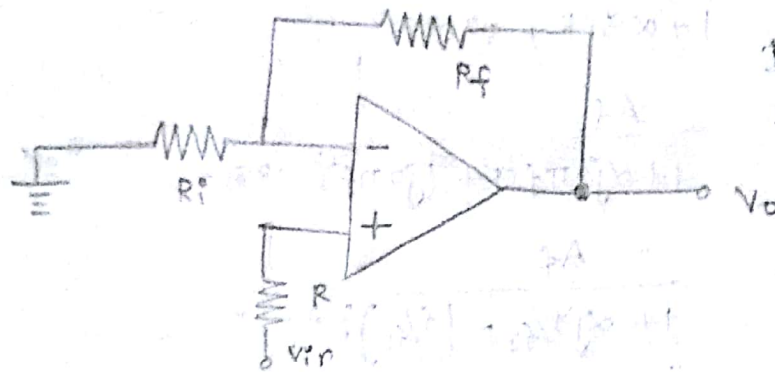
$$\frac{V_b}{R} + \frac{V_b - V_o}{R} = 0$$

$$2V_b - V_o = 0$$

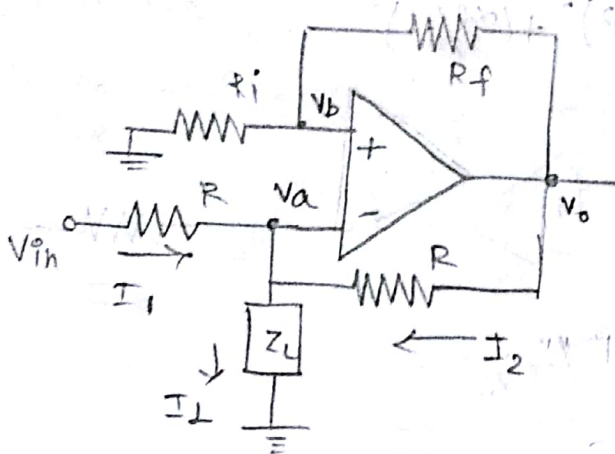
$$2V_b = V_o$$

$$\boxed{V_b = \frac{V_o}{2}} \quad \text{--- (2)}$$

V-I converter other name is trans conductance amplifier. A non-inverting amplifier is an voltage to current converter.



V-I using floating load.



Apply node equation on a,

$$\frac{V_a - V_i}{R} + \frac{V_a - V_o}{R} + I_L = 0$$

$$\frac{V_a - V_i}{R} + \frac{V_a - V_o}{R} = -I_L$$

$$V_a - V_i + V_a - V_o = -I_L R$$

$$2V_a = V_i + V_o - I_L R$$

$$V_a = \frac{V_i + V_o - I_L R}{2} \quad \text{--- (1)}$$

$$A = 1 + \frac{R_f}{R_i}$$

$$R_f = R_i = R$$

$$A = 1 + \frac{R}{R} = 1 + 1$$

$$\boxed{A = 2}$$

$$\frac{V_o}{V_i} = 2$$

$$V_o = 2V_i$$

Apply node equation on node b,

$$\frac{V_b}{R_i} + \frac{V_b - V_o}{R_f} = 0$$

$$R_i = R_f = R$$

$$\frac{V_b}{R} + \frac{V_b - V_o}{R} = 0$$

$$2V_b - V_o = 0$$

$$2V_b = V_o$$

$$\boxed{V_b = \frac{V_o}{2}} \quad \text{--- (2)}$$

equation (1) & (2)

$$V_a = V_b$$

$$\frac{V_i + V_o - I_L R}{2} = \frac{V_o}{2}$$

$$\frac{V_i}{2} + \frac{V_o}{2} - \frac{I_L R}{2} = \frac{V_o}{2}$$

$$\frac{V_i}{2} = \frac{I_L R}{2}$$

$$I_L = \frac{V_i}{R}$$

Applications:

- (1) Used in DC and AC Voltmeter
- (2) Used in LED and Zener diode test

JFET → Voltage control current source

BJT → current controlled current source

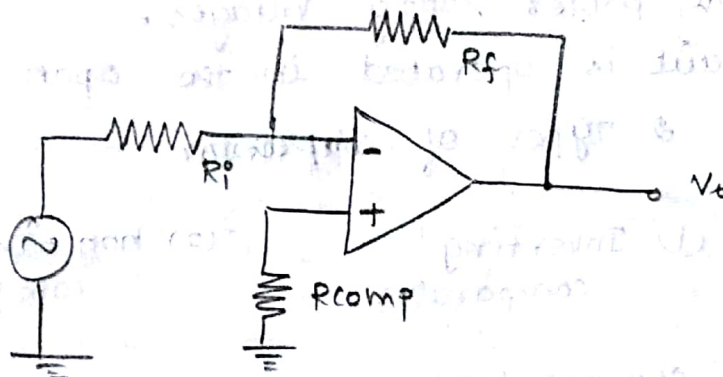
Current to voltage converter:

$$T_{OS} \left(1 - \left(\frac{V_{OS}}{V_P} \right)^2 \right)$$

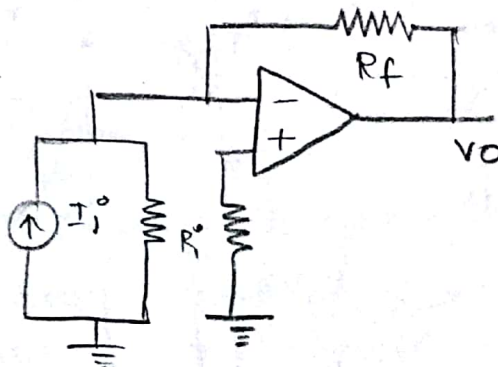
I to V converter other name is transresistance.

An Inverting amplifier act as I to V converter.

A current source is parallel with resistor can be replaced as a voltage source is series with resistor.



I to V converter,



* Photo cell, photo transistor gives the o/p as current is proportional to incident light.

* This I to V converter measures the small amount of current and convert that to measurable voltage.

Notes:

The capacitor CF can be shunted with RF to reduce high frequency noise.

2/2/18

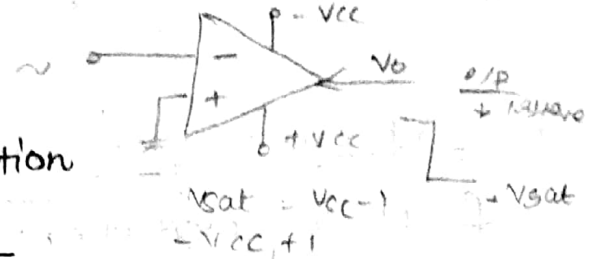
COMPARATOR

$A = \infty$
o/p saturated ZL

note:

In open loop configuration

$A = \infty \rightarrow$ output saturated Z
($\pm V_{CC} \mp 1$)



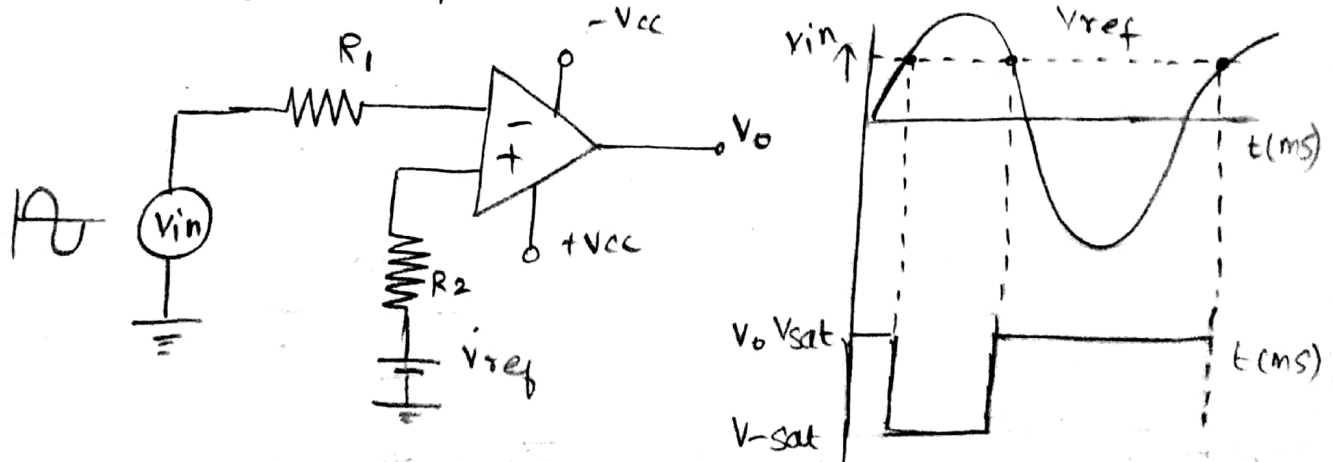
A comparator compares the two inputs and gives out the output as square wave its amplitude is decided by the power supply voltages.

This circuit is operated in the open loop configuration. 2 types of comparator.

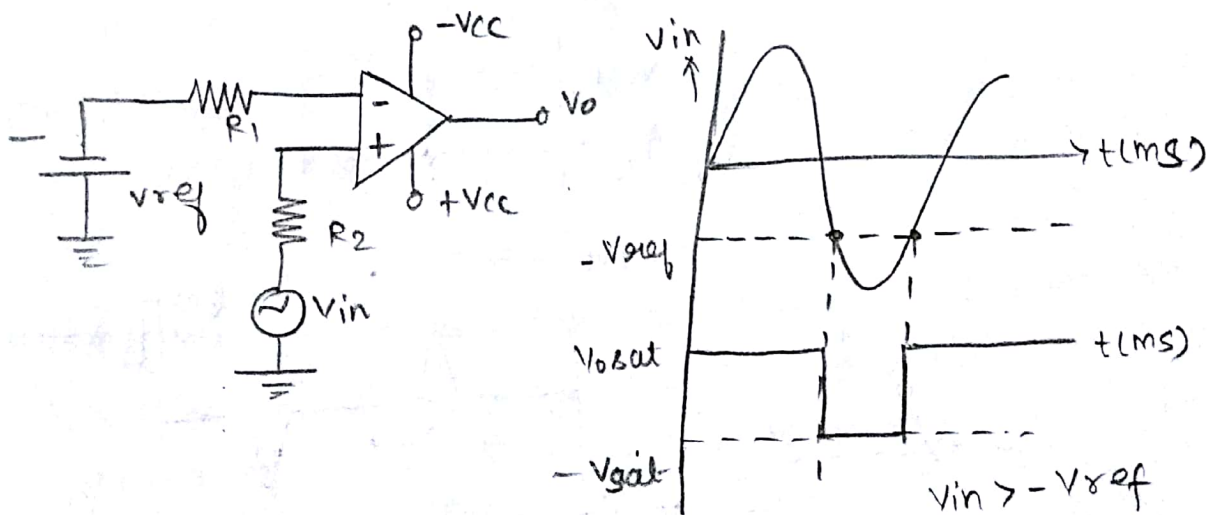
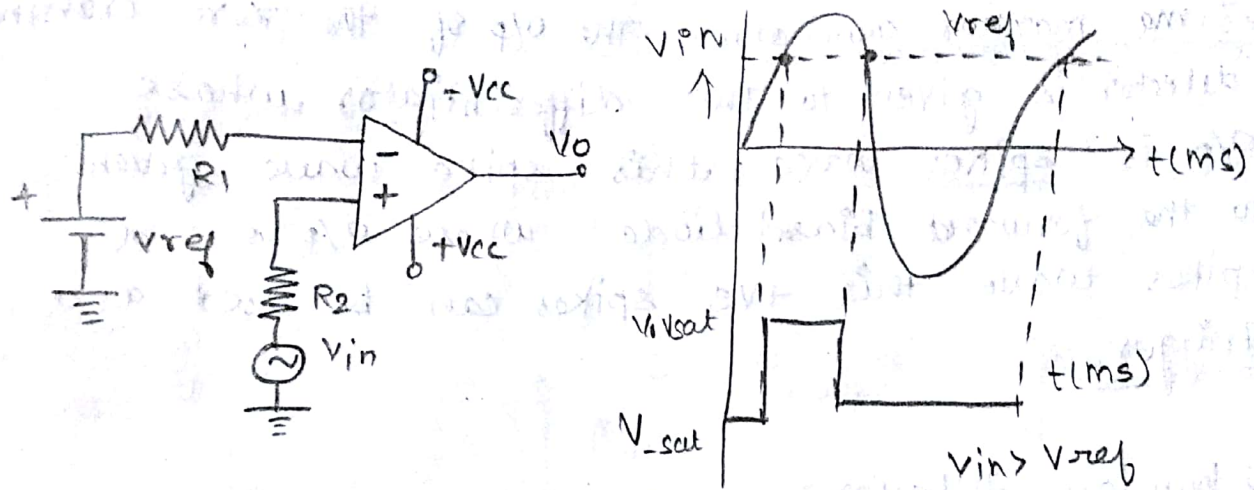
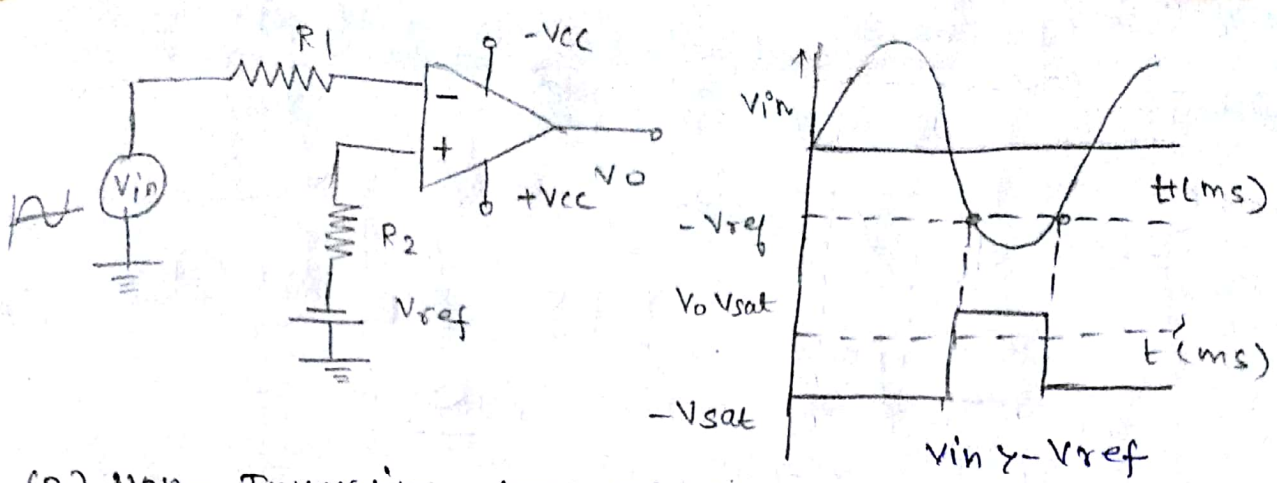
(1) Inverting comparator

(2) non-Inverting comparator

(1) Inverting comparator:



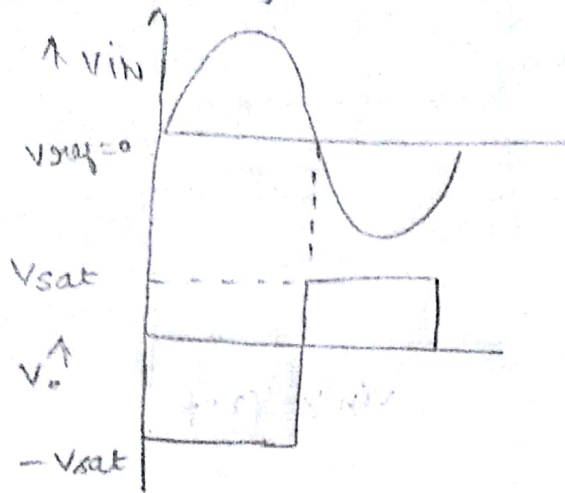
when $V_{in} > V_{ref}$



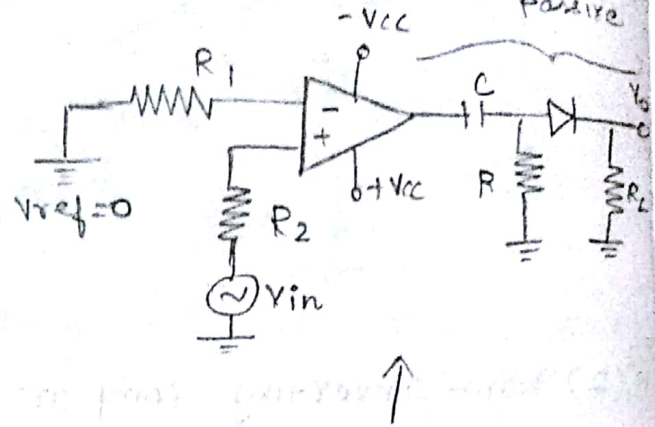
Applications:

- ① (1) Zero Crossing detector: $-V_{ref} = 0$, so compare 2 input $1 \rightarrow \sin \gamma \rightarrow$
- 2m Detects whenever the input changes from +ve to -ve cycle in this circuit $V_{ref} = 0$ for +ve half cycle output is OFF and for -ve half cycle output is ON.

Zero crossing detector:

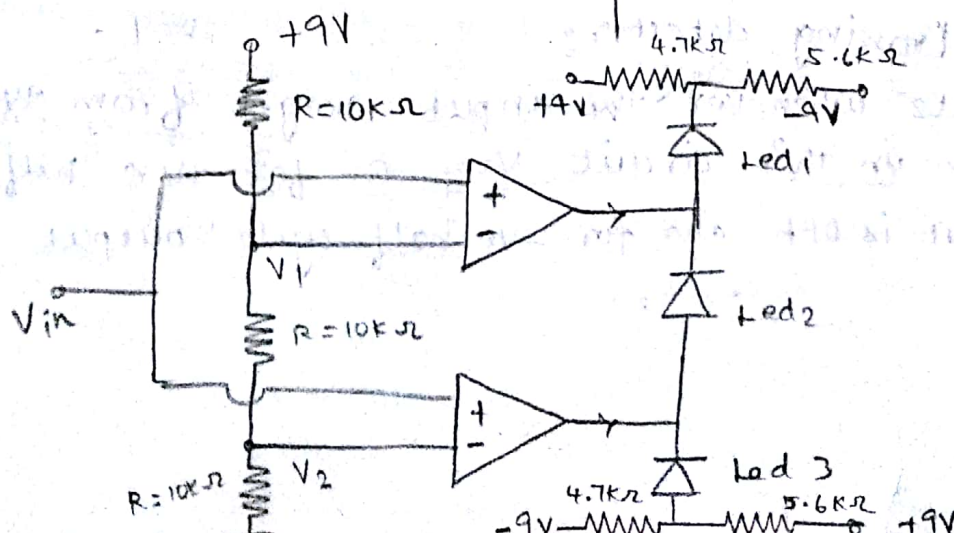
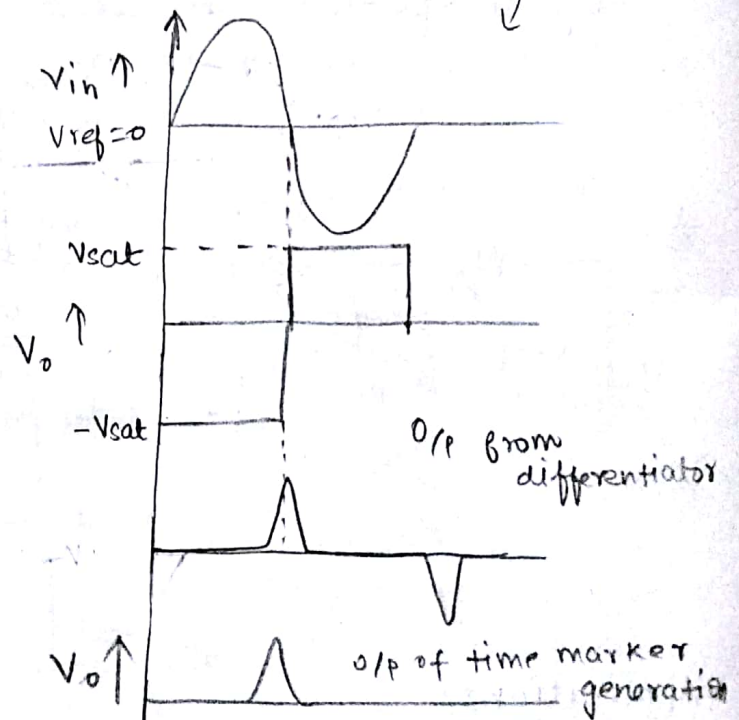


Time marker generator



1) Time marker generator: The o/p of the zero crossing detector is given to the differentiator whose o/p is spikes wave, this spike wave given to the forward biased diode whose o/p is a spikes wave this +ve spikes can be used as a trigger. (normal to abnormal) state

3) Window Detector:
(Voltage level indicator)



Op-Amp circuits Using Diodes

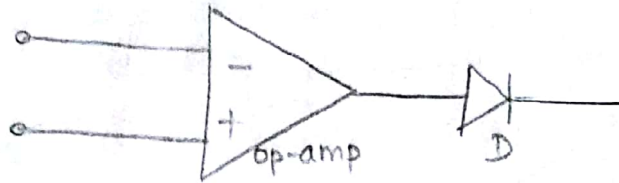
- 1) clipper
- 2) clamper
- 3) peak Detector
- 4) Rectifier → HWR
→ FWR

adv's
cut off voltage
to millivolt
↓
when we
combine
op-amp &
diode

Precision Diode:

It is the combination of op-amp and Pn diode
the advantage of this is the cut off frequency is
very less (ie) in millivolt, comparatively a normal
diode has 0.7V.

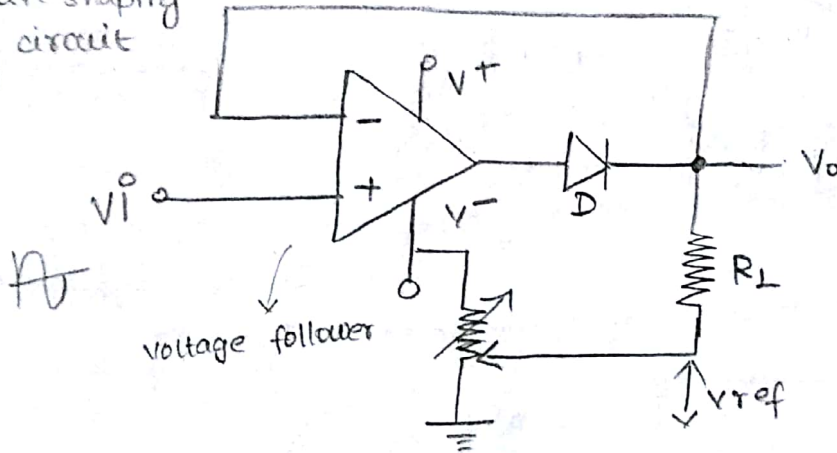
Precision Diode



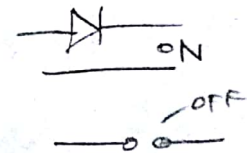
Clipper:

wave shaping
circuit

(1)



Diode → act as switch

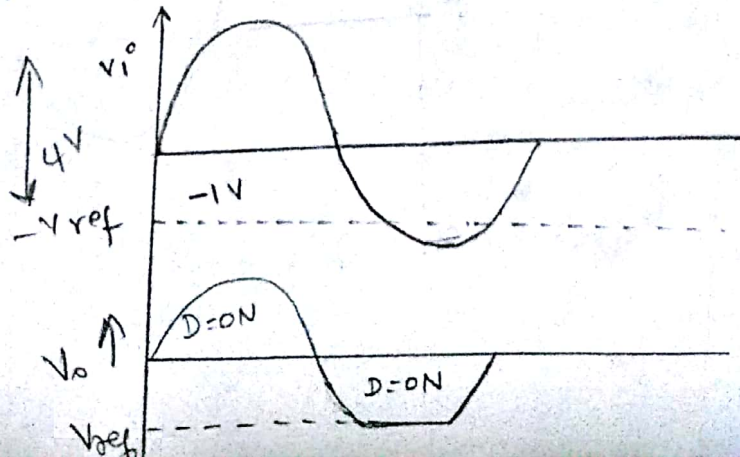


Allow the wave
or reject the wave
↓
use of the diode

The above clipper has an voltage follower with
a precision diode, There is only a stage

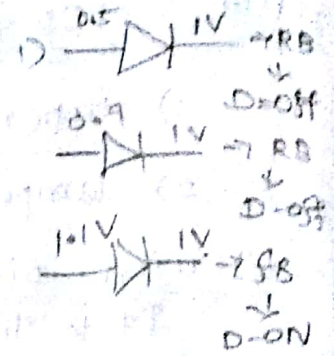
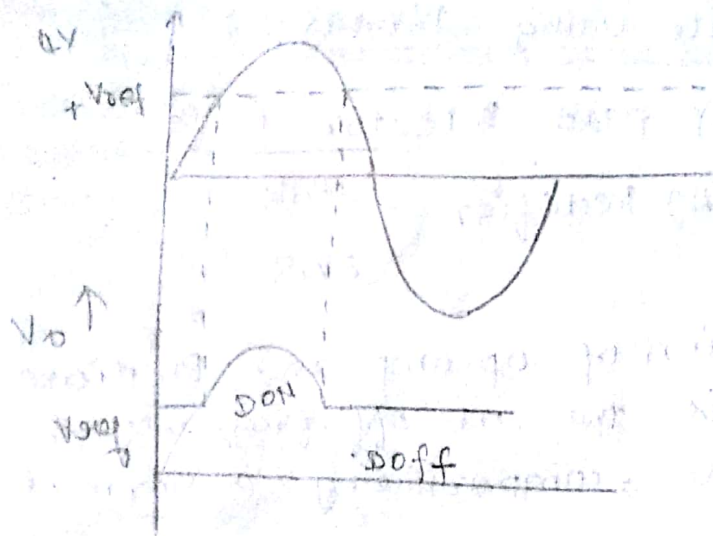
(1) when the Diode is Forward bias, Input
appears at the output.

(2) when the Diode is Reverse biased, input is
clipped off.



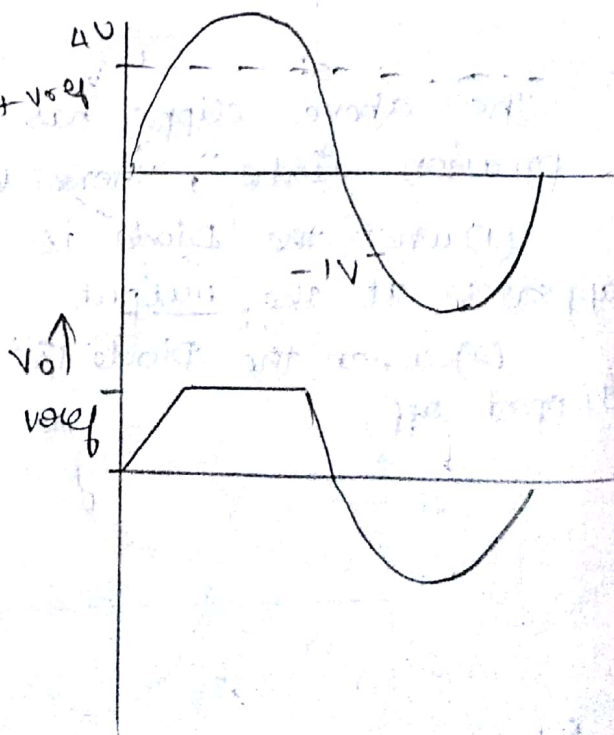
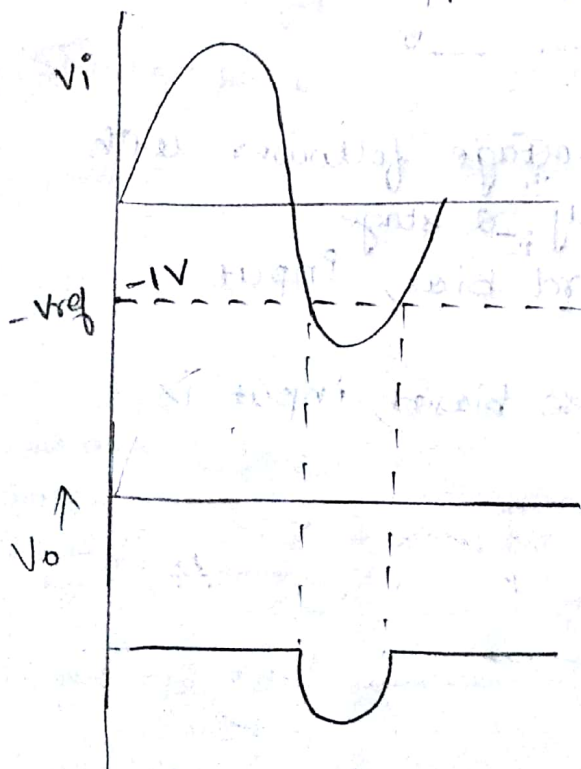
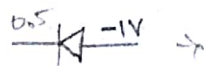
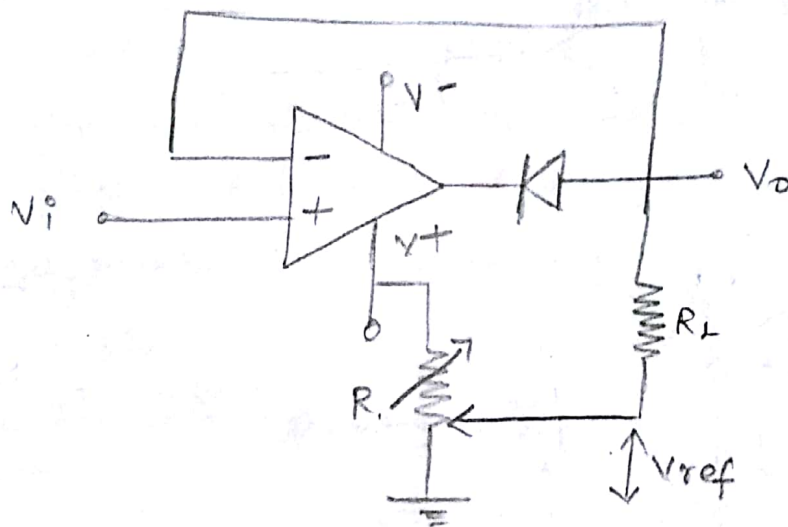
depending upon the
applied voltage

1) 0.5V → ON
FB
(2) -1.0V → OFF
RB



-ve clipper (it clip -ve portion)

(Q)



-ve clipper:

$-V_{ref}$

- (1) $V_i > -V_{ref}$, Di is FB $\rightarrow$ ON
output follows input,
- (2) $V_i < -V_{ref}$, Di is RB $\rightarrow$ OFF
output is $-V_{ref}$ (DC value)

+ve clipper:

$-V_{ref}$

- (1) $V_i < -V_{ref}$, Di is FB $\rightarrow$ ON
output follows input
- (2) $V_i > -V_{ref}$, Di is RB $\rightarrow$ OFF
output is $-V_{ref}$ (DC value)

$+V_{ref}$

- (1) $V_i > V_{ref}$, Di is FB $\rightarrow$ ON
o/p follows input
- (2) $V_i < V_{ref}$, Di is RB $\rightarrow$ OFF
output is $+V_{ref}$

$+V_{ref}$

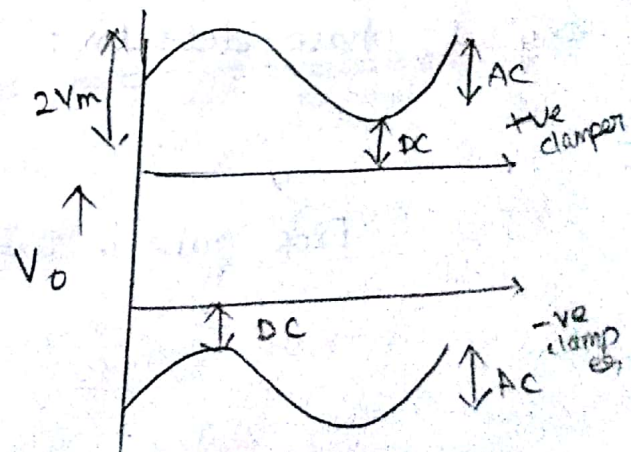
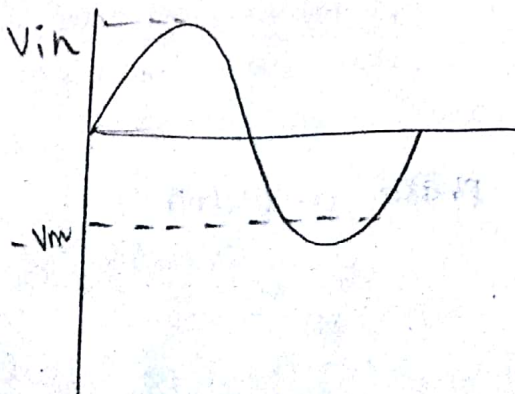
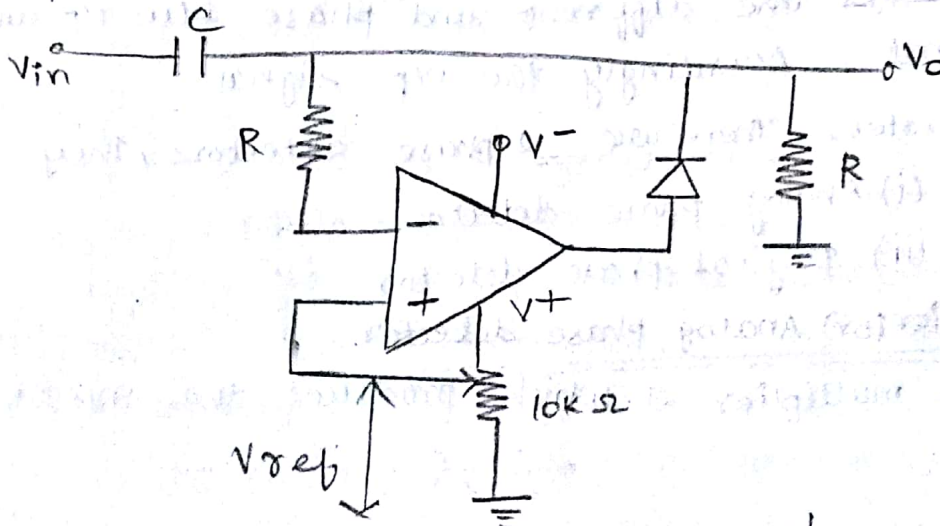
- (1) $V_i < V_{ref}$, Di is FB $\rightarrow$ ON
- (2) $V_i > V_{ref}$, Di is RB $\rightarrow$ OFF

CLAMPER

along v

(DC inserter or Restorer)

- 1) Along with AC, DC is inserted
- 2) Voltage follower along with Diode, and capacitor at input.



6/12/18

UNIT-III Analog multiplier and PLL

PLL - Phase locked loops - used in AM & FM

IC → used in no communication purpose

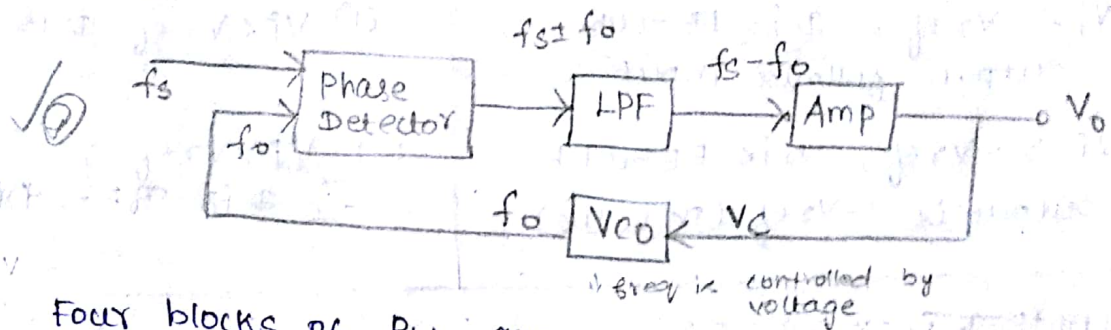
noise will affect voltage in AM

PLL is used in the communication field when there is shift in the frequency of the signal

PLL is used to synchronise the frequency and phase of i/p and o/p.

Block Diagram:

angle freq / phase freq
varies with time



Four blocks of PLL are,

- (1) Phase detector
- (2) Low pass filter
- (3) Amplifier
- (4) VCO

Phase detector:

It detects the difference and phase b/w i/p and o/p of the signal. Accordingly the o/p signal $fs \pm fo$ is generated. There are 2 phase detectors, they are

- (i) Analog phase detector → a mult
- (ii) Digital phase detector

Analog multiplier (or) Analog phase detector

It is a multiplier which produces the mixture of fs, fo .

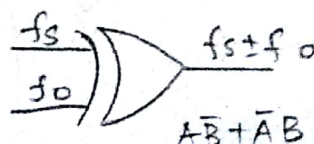
Digital phase detector:

both i/p equal o/p be 1

00 → 1
11 → 1

square wave - XOR gate
sine wave - multiplier

XOR gate is used as a phase detector.



truth table for

$S(fs)$	$S(fo)$	$S(fs \oplus fo)$	XOR
0	0	0	
0	1	1	
1	0	1	
1	1	0	

Low Pass filter:

LPF filters out $f_s + f_o$ frequency component and allows only $f_s - f_o$ low frequency component.

Amplifier:

The voltage of $f_s - f_o$ signal is amplified and its voltage V_c is given to V_{CO}

Voltage control oscillator (V_{CO})

Output frequency f_o changes with the input voltage.

PLL has 3 states:

(i) Free Running state

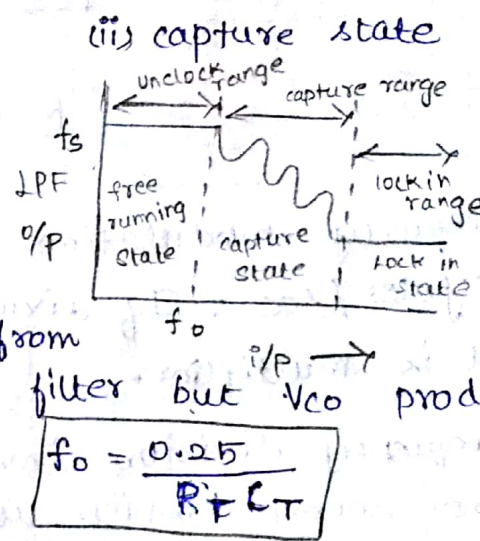
(ii) capture state

(iii) Lock in state

(1) FREE RUNNING STATE:

When no input is given to PLL, no output from phase detector and low pass filter but V_{CO} produces its own free running frequency

$$V_c = \frac{1}{8} V_{CC}$$



(2) CAPTURE STATE:

The input signal frequency $f_s \neq f_o$. Hence we need to capture the frequency f_s .

Now the value V_c changes according to the difference in freq. $f_s - f_o$ and the o/p frequency correspondingly.

This continues until f_o capture f_s .

(3) LOCK IN STATE:

$$f_s = f_o,$$

when PLL enter into lock in state

(e) PLL can track any change in incoming freq here after

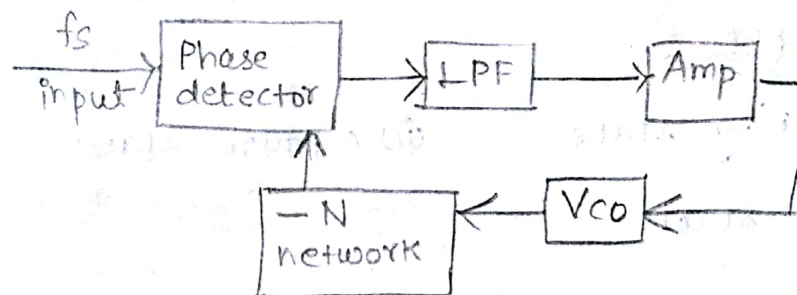
The range over which the freq. is locked is called lock in range.

Application of PLL:

- Frequency multiplication / division
- Frequency translation
- AM detection
- FM demodulation
- FSK demodulation
- freq shift key

$2m, 2n$
↓
application of PLL

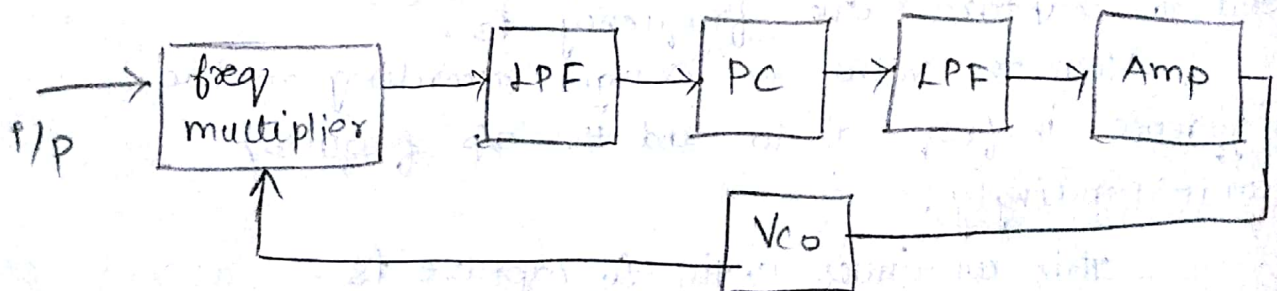
1) Frequency multiplication / Division.



Frequency modulation involves increasing the no. of cycles/sec. If divide by n - network is used. It is multiplier.

Frequency division involves decreasing the cycles per second which use $1/n$ network

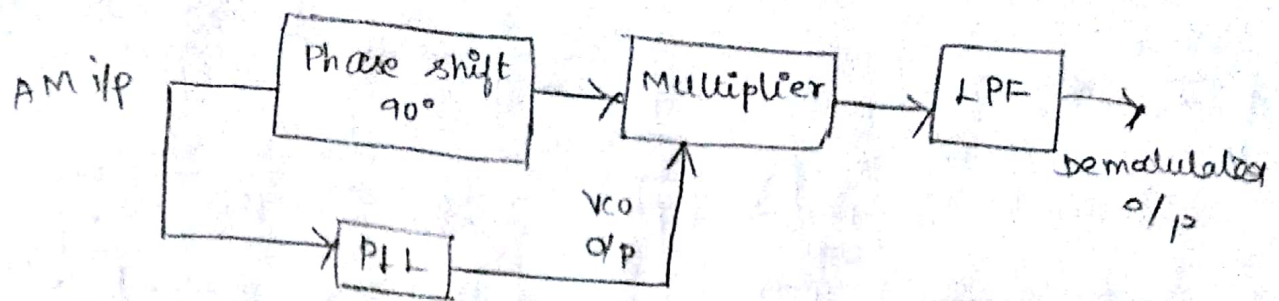
9/2/18 2) Frequency Translation:



$$b/p \quad f_o = f_s + f_i$$

Add some frequency.

3) AM detection:



PLL is locked to carrier frequency of the AM signal. Under locked condition the AM signal shifted by 90° fed to the multiplier.

The o/p of multiplier contains both sum & difference which is pass through the LPF to ^{which filters} eliminate the high frequency components.

Advantages :

- 1) selectivity
- 2) Noise immunity is better than ^{tracks the freq}

4) FM demodulation :

If PLL locked to FM signal VCO tracks the instantaneous frequency of i/p signal.

The error voltage controls the VCO and the PLL locked to the i/p signal of FM o/p.

5) Frequency shift key demodulation (FSK) → eg: MODEM computers

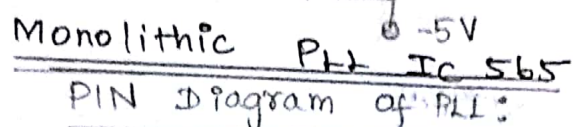
Convert digital → analog.

In digital data communication binary data is transmitted by means of a presets frequency for '1' and '0' this is called FSK technique.

operation:

As the signal appears at the i/p PLL tracks the frequency of the i/p signal b/w 2 frequencies, with corresponding shift in the o/p.

This section is followed by RC ladder filter which removes the carrier and produces the digital o/p.



$$f_{\text{lock}} = \frac{8 \cdot f_{\text{out}}}{V} \text{ (Hz)}$$

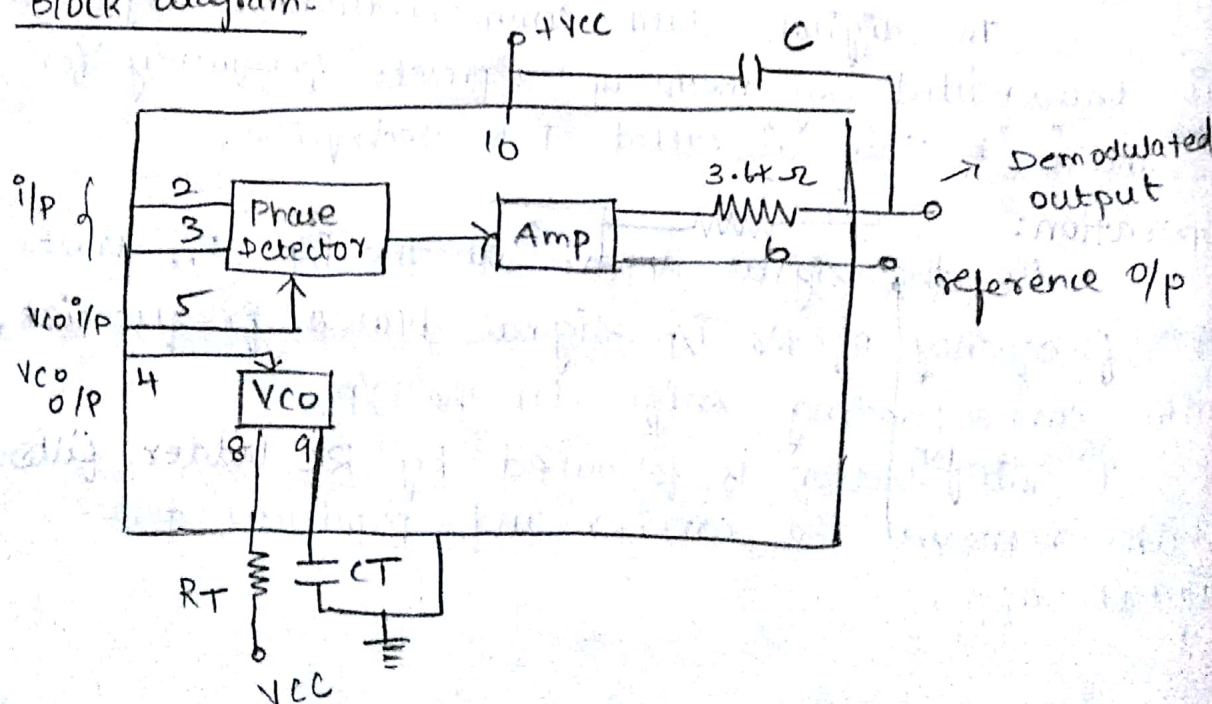
$$f_c = \frac{1}{2\pi(3.6k)(2)} \sqrt{2}$$

-Vcc	1	14	NC
i/p	2	13	NC
i/p	3	12	NC
Vco O/p	4	11	NC
Phase comp Vco i/p	5	10	+Vcc
Reference V/p	6	9	external C for Vco
Demodulated o/p	7	8	external R for Vco

NE/SE
565

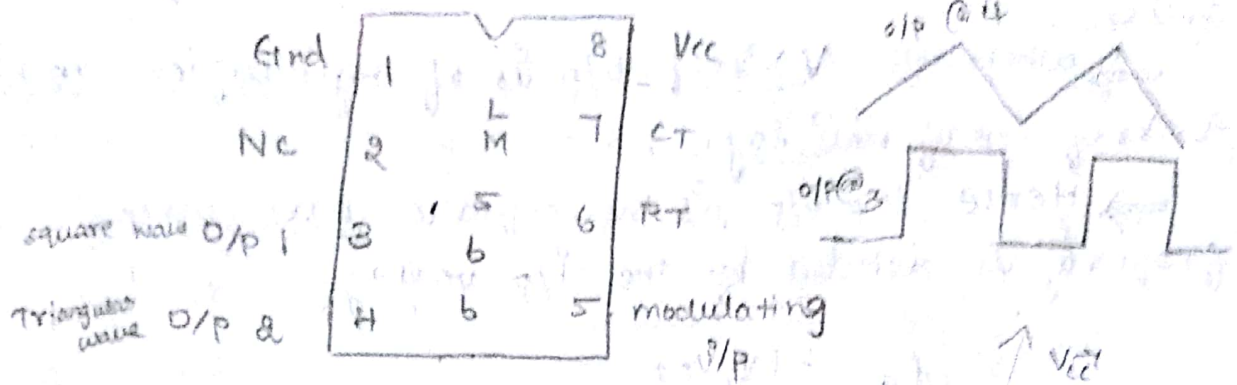
$f_c = \frac{1}{T}$
capture freq

Block diagram:

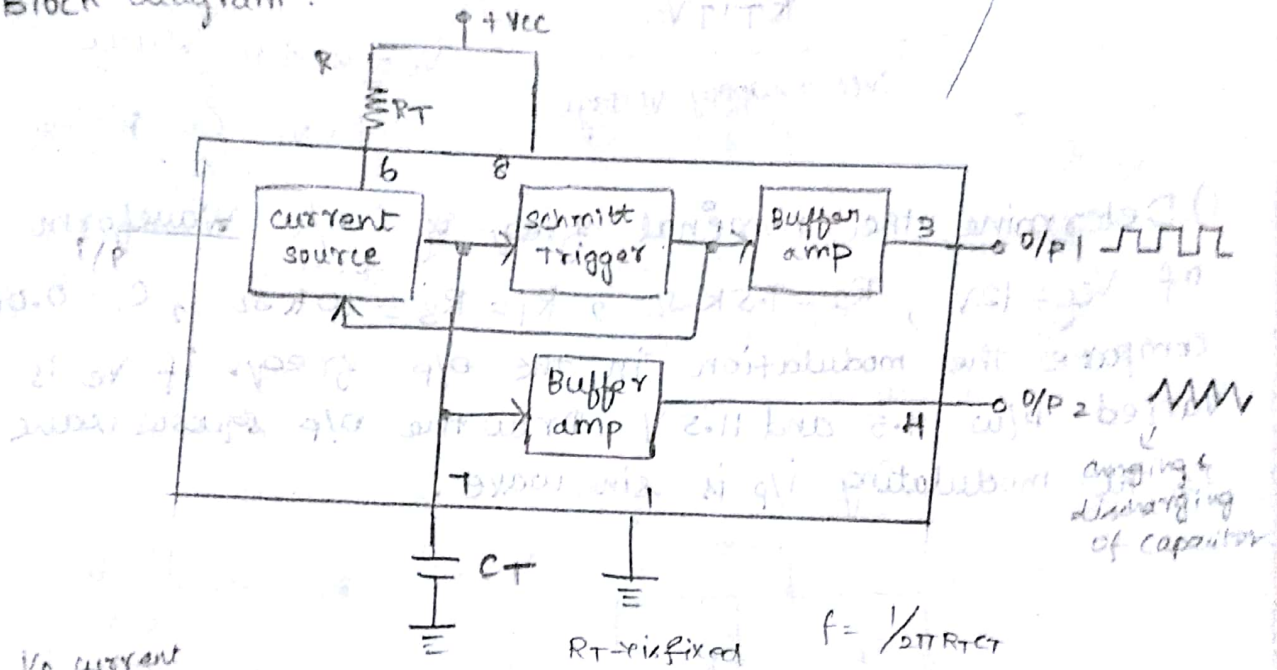


10/2/17

VCO:



Block diagram:



V_o current charges the CT and freq. also changes amplitude is decided by CT

VCO: * The o/p can be changed by over a wide range of frequency by applied modulating i/p signal.

* The current sources converts the voltage to current so that the capacitor charges accordingly, the capacitor voltage increases gradually.

* which gives triangular wave o/p at pin no. 4 (charging and discharging of CT).

When the modulating i/p is applied to the Schmitt Trigger (Regenerative comparator).

→ Whose V_{ref} is decided by the o/p V_o through a resistor network which acts as the reference voltage.

→ whenever $V > V_{ref}$ o/p is of High logic and $V < V_{ref}$ o/p of Low logic.

→ Hence the o/p is the square wave whose frequency is decided by the i/p voltage.

$$f = \frac{2(V_c - V_c)}{R_T C_T V_{cc}}$$

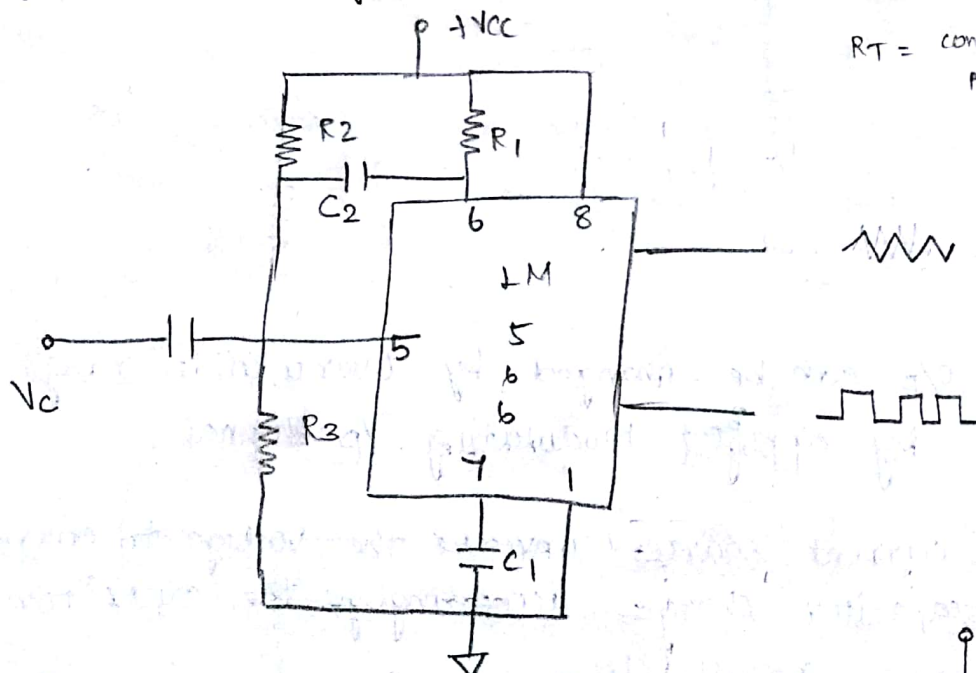
V_{cc} → supply voltage

V_c → control voltage

f ∝ V_c @ pin no. 5

problem on PLL

- 1) Determine the nominal freq. of o/p waveform of $V_{cc} = 12V$, $R_2 = 1.5K\Omega$, $R_1 = R_3 = 10K\Omega$, $C_1 = 0.001\mu$ compute the modulation in the o/p freq. if V_c is varied b/w 9.5 and 11.5V. Draw the o/p square wave if the modulating i/p is sine wave.

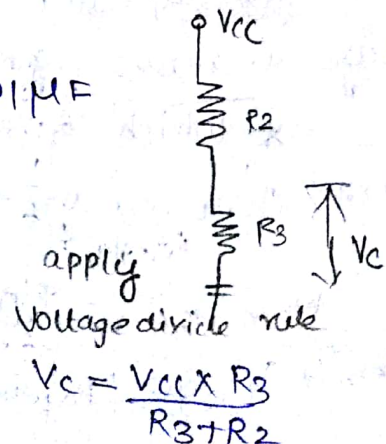


R_T = connected b/w pin 6 & 7

$R_T = 10K\Omega$

$C_T = 0.001\mu F$

$$f = \frac{2(V_{cc} - V_c)}{R_T C_T V_{cc}}$$



$$V_c = \frac{V_{cc} \times R_3}{R_3 + R_2}$$

$$V_c = \frac{12V \times 10K}{(10K + 15K)} = 10.434$$

$$f = \frac{2 \left(\frac{12}{V_c} - 10.434 \right)}{(10K\Omega)(0.001\mu F)(12)} = \frac{3.1304}{1.2 \times 10^{-4}} = 26.0866$$

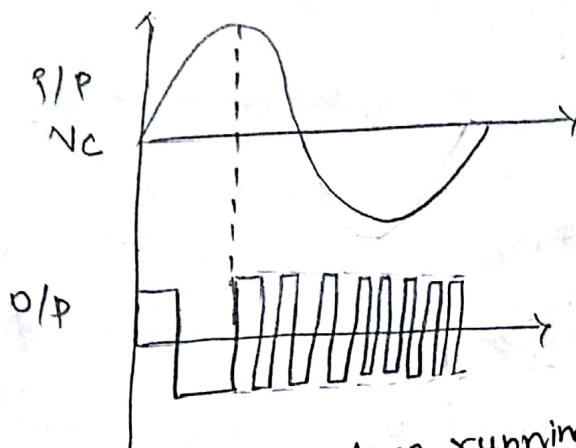
(i) $V_c = 9.5$

$$f = \frac{2(12 - 9.5)}{1.2 \times 10^{-4}} = \frac{5}{1.2 \times 10^{-4}} = 41.66 KHz$$

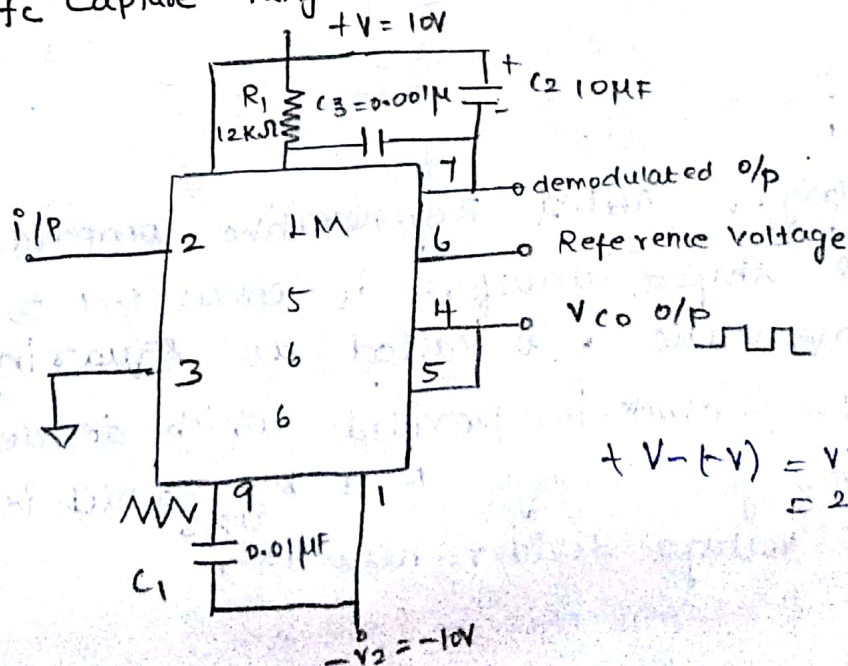
(ii) $V_c = 11.5V$

$$f = \frac{2(12 - 11.5)}{1.2 \times 10^{-4}} = 8.33 KHz$$

When voltage $\uparrow$ the frequency of oscillation $\downarrow$
 $V_c \propto 1/f \propto T(V_c)$



2) Determine the free running freq. f₀ of PLL in range f_c capture range f_c of PLL:



$$+V - (-V) = V + V = 2V$$

$$f_{out} = \frac{1.2}{4RC} \text{ Hz} = \frac{1.2}{4(12k\Omega)(0.01\mu)} = 2500$$

$$= 2.5 \text{ KHz}$$

$$f_L = \frac{8(2.5 \text{ KHz})}{20} = 1000 \text{ Hz}$$

$$f_c = \pm \left[\frac{f_L}{2\pi(3.6k)(2)} \right]^{1/2} = \pm \left[\frac{1000}{2\pi(3.6k)(2)} \right]^{1/2}$$

$$= \pm \left[\frac{1000}{0.2261} \right]^{1/2}$$

$$= \pm [4422.82]^{1/2}$$

$$= \pm 66.504 \text{ Hz}$$

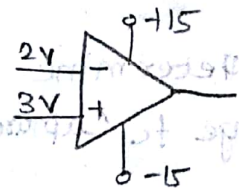
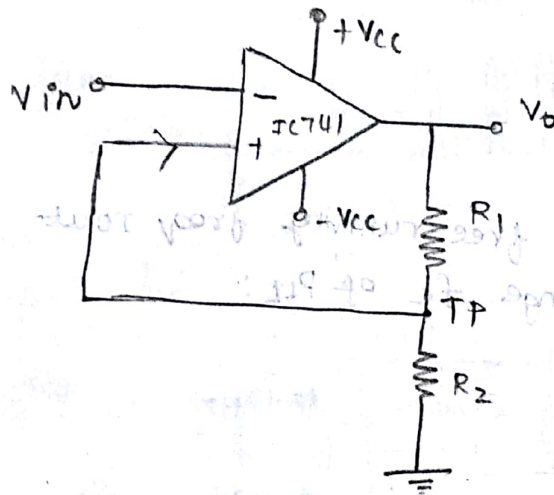
Unit - II

SCHMITT TRIGGER

(Regenerative comparator):

o/p be a perfect square wave even if the i/p is not a perfect sine wave)

BP
3A



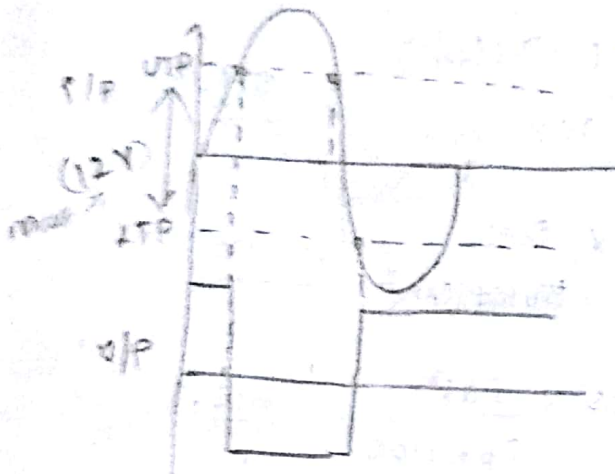
Schmitt Trigger called Regenerative comparator if any irregular shaped waveform is converted to a perfect square wave, is called as squaring circuit. The feedback is provided which decides the threshold voltage through R_1 & R_2 which is nothing but voltage divider network.

2 Threshold points - UTP & LPT

Two Threshold voltage: $\begin{cases} \text{upper threshold voltage (UTP)} \\ \text{Lower threshold voltage (LTP)} \end{cases}$

$$V_{UT} = V_{CC} \times \frac{R_2}{R_1 + R_2}$$

$$V_{LT} = -V_{CC} \times \frac{R_2}{R_1 + R_2}$$



Whenever the sine wave cut the UTP, LTP, the square wave changes.

Hysteresis loop

Whenever the i/p voltage exceeds the threshold point there will be state change in the o/p.

It is $V_{in} > V_{UT}$ o/p square wave changes from ON to OFF.

When $V_{in} > V_{LT}$ o/p changes from OFF to ON

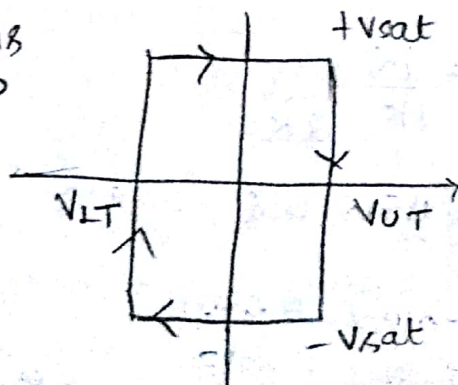
The comparator with the feedback exhibits hysteresis i.e.) when the i/p exceeds the threshold point the o/p changes its state and given reversed back to the original state when reaches the other threshold point.

$$V_h = V_{UT} - V_{LT}$$

$$= \frac{V_{CC} R_2}{R_1 + R_2} - \left(-\frac{V_{CC} R_2}{R_1 + R_2} \right)$$

$$V_h = \frac{2 V_{CC} R_2}{R_1 + R_2}$$

Hysteresis loop

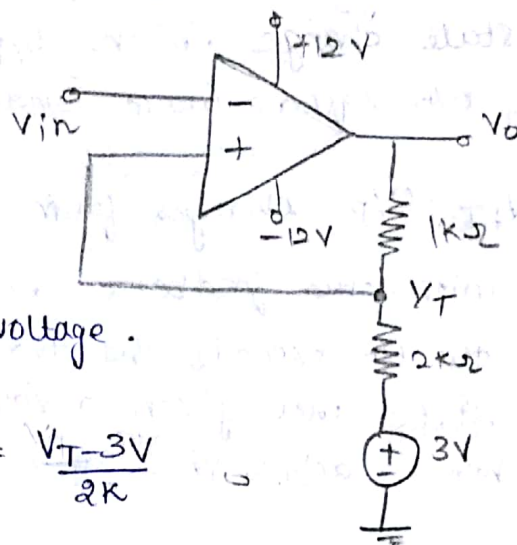


1) Determine the UT & LT of Schmitt Trigger with a circuit supply voltage $\pm 15V$ $R_1 = 100\Omega$ $R_2 = 56k\Omega$ V_{TP} voltage = $1V$. find the Hysteresis Voltage.

$$V_h = \frac{2V_{cc} R_2}{R_1 + R_2} = \frac{2(15)(56k)}{100 + 56k} = \underline{29.946}$$

$$V_{UT} = V_{cc} \times \frac{R_2}{R_1 + R_2} = 15 \times \frac{56k}{56k + 100} = \underline{14.97}$$

$$V_{LT} = -V_{cc} \times \frac{R_2}{R_1 + R_2} = -15 \times \frac{56k}{56k + 100} = \underline{-14.97}$$



find UTP & LTP

Apply node voltage .

$$\frac{V_o - V_T}{1k} = \frac{V_T - 3V}{2k}$$

$$\frac{V_o - V_T}{1k} = \frac{V_T - 3V}{2k}$$

$$\frac{12 - V_T}{1k} = \frac{V_T - 3V}{2k}$$

$$\frac{12k - V_T}{1k} = \frac{V_T - 3V}{2k}$$

$$\left(\frac{V_T}{2k} + \frac{V_T}{1k} \right) = \frac{12}{1k} + \frac{3V}{2k}$$

$$V_T \left(\frac{1}{2k} + \frac{1}{1k} \right) = 0.012 + 0.0015$$

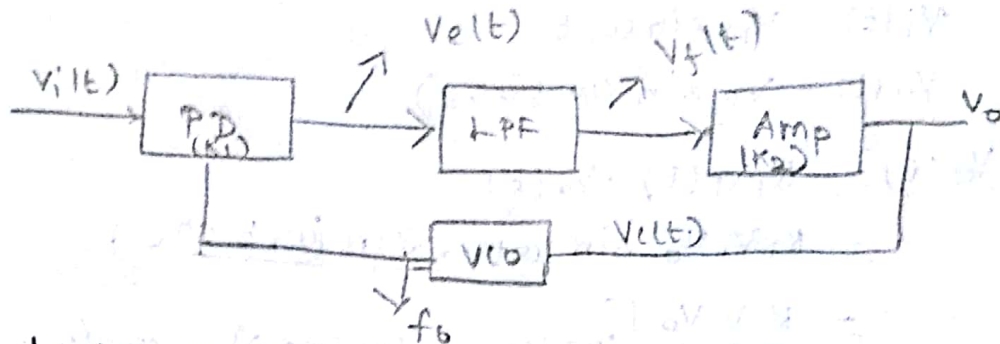
$$V_T (1.5 \times 10^{-3}) = 0.013$$

$$V_T = \frac{0.013}{1.5 \times 10^{-3}} = \underline{8.6 \approx 9}$$

Analysis of PLL:

The operation of PLL is verified using mathematical expression consider i/p will be,

$$V_i(t) = V_i \sin \omega t$$



case 1:

Unlocked state:

$$V_i(t) \neq V_o(t)$$

during this state o/p V_o , generate its own frequency f_0 . Under this state PLL is unlocked therefore error voltage $V_e(t)$ is,

$$V_i(t) = V_i \sin \omega t$$

$$V_o(t) = V_o \sin \omega_0 t$$

$$V_e(t) = K_1 V_i(t) \cdot V_o(t)$$

$$= K_1 V_i \sin \omega_1 t \cdot V_o \sin \omega_0 t$$

$$= K_1 V_i V_o \sin \omega_1 t \sin \omega_0 t$$

$$\frac{\sin A}{\sin B} = \frac{\cos(A-B) - \cos(A+B)}{2}$$

$$V_e(t) = K_1 \frac{V_i V_o}{2} \left[\cos(\omega_1 - \omega_0)t - \cos(\omega_1 + \omega_0)t \right]$$

low pass filter
It only passes two

This signal $V_e(t)$ passed through low pass filter which filter the sum frequency, then o/p be

$$V_f(t) = K_1 \frac{V_i V_o}{2} \cos(\omega_1 - \omega_0)t$$

o/p frequency voltage under unlocked state

$$V(t) = \frac{K_1 K_2 V_i V_o}{2} \cos(\omega_1 - \omega_0)t$$

K_1 - gain of the phase detector

K_2 - gain of the amplifier

Case 2:

Locked state:

Under locked state, $f_o = f_i$

$$V_i(t) = V_o(t)$$

$$V_i(t) = V_i \sin \omega_i t$$

$$V_o(t) = V_o \sin(\omega_i t + \theta_e)$$

$$V_e(t) = K_1 V_i(t) \cdot V_o(t)$$

$$= K_1 V_i V_o \sin \omega_i t \cdot \sin(\omega_i t + \theta_e)$$

$$= \frac{K_1 V_i V_o}{2} \left[\cos(\omega_i t - (\omega_i t + \theta_e)) - \cos(\omega_i t + (\omega_i t + \theta_e)) \right]$$

$$= \frac{K_1 V_i V_o}{2} \left[\cos(-\theta_e) - \cos(2\omega_i t + \theta_e) \right]$$

↓ filtered by
LPF

$$V_e(t) = \frac{K_1 V_i V_o}{2} \cos(-\theta_e)$$

$$V(t) = \frac{K_1 K_2 V_i V_o}{2} \cos(-\theta_e) \rightarrow \text{o/p voltage for locked state}$$

1) Expression for lock-in-range:

does not affect LPF gain

Let consider the o/p voltage of phase detector,

$$V_e = K_1 (\phi - \pi/2)$$

K_1 - gain of phase detector

ϕ - phase difference b/w f_i & f_o

During lock-in-range $f_i = f_o$,

∴ the final voltage V_o after low pass filter and amplifier

$$V_c = V_o = \frac{K_1 K_2 (\phi - \pi/2)}{\downarrow \text{gain of amplifier}} \quad \text{--- (1)}$$

Now, this V_o is applied to V_{co} as a control voltage V_c which shifts the free-running freq f_o to a new frequency f .

$$f = f_0 + K_V V_c$$

K_V - gain of the V_{CO}

$$V_c = \frac{f - f_0}{K_V}$$

under locked state, $f = f_s$

$$\therefore V_c = \frac{f_s - f_0}{K_V} \quad \text{--- (2)}$$

equate (1) & (2)

$$K_1 K_2 (\phi - \pi/2) = \frac{f_s - f_0}{K_V}$$

$$\text{lock-in-range frequency} \leftarrow f_s - f_0 = K_1 K_2 K_V (\phi - \pi/2)$$

$$\Delta f_L = K_V K_1 K_2 (\phi - \pi/2) \quad \text{--- (3)}$$

If the phase shift $(\phi - \pi/2) = \pi/2$

$$\Delta f_L = \frac{K_V K_1 K_2 \pi}{2}$$

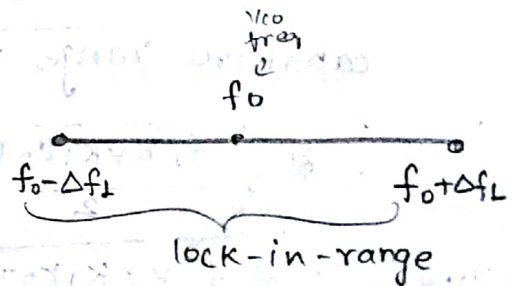
The frequency over which PLL can be locked will be $2 \Delta f_L$

Now sub Δf_L ,

$$= \cancel{2} \left[\frac{K_V K_1 K_2 \pi}{\cancel{2}} \right]$$

$$\text{lock-in-range} = K_1 K_2 K_V \pi$$

Difference b/w $\phi + \pi$



2) Expression for capture Range:

under capture state $f_1 \neq f_0$,

Hence the o/p after LPF,

$$V_o = A K_1 K_2 (\phi - \pi/2) \quad \text{--- (1)}$$

$$V_c = \frac{f_s - f_0}{K_V} \quad \text{from previous (2)}$$

the gain of the LPF,

$$A = \frac{1}{\sqrt{1 + (f/f_L)^2}} = \frac{1}{\sqrt{(f/f_L)^2}} = f_L/f$$

$$f/f_L \gg 1$$

$$A = f_L/f \quad \text{--- (3)}$$

sub (3) in (1)

$$V_c = V_o = \frac{f_L}{f} K_1 K_2 (\phi - \pi/2) \quad \text{--- (4)}$$

$f_L \rightarrow$ cut-off freq of LPF

equating (4) & (2)

$$\frac{f_s - f_o}{K_V} = \frac{f_L}{f} K_1 K_2 (\phi - \pi/2)$$

$$f = f_s - f_o = K_V K_1 K_2 (\phi - \pi/2) \frac{f_L}{f}$$

consider $\phi = \pi$

$$f^2 = \frac{f_L K_V K_1 K_2 \pi}{2}$$

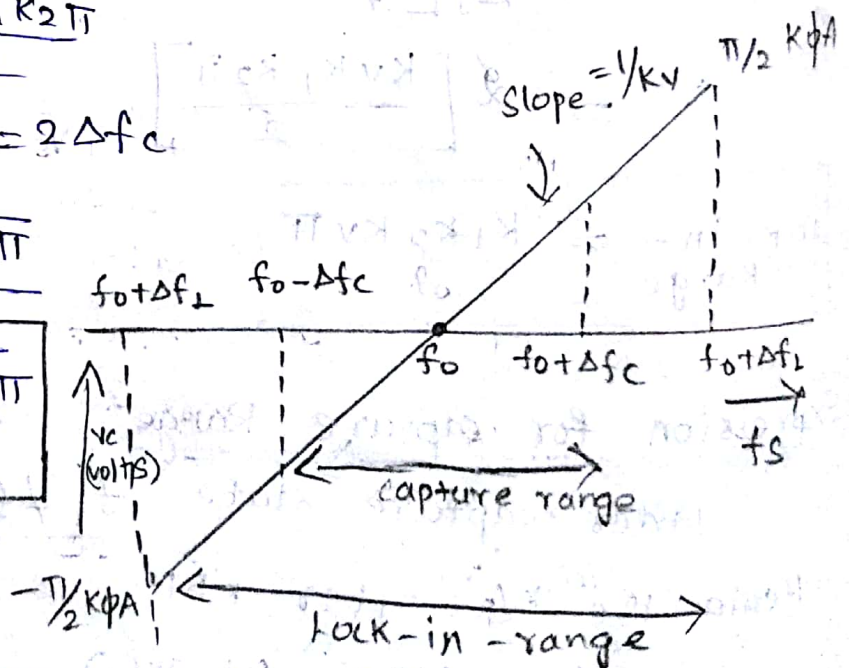
capture range

$$\Delta f_c = \sqrt{\frac{f_L K_V K_1 K_2 \pi}{2}}$$

$$\text{capture range} = 2 \Delta f_c$$

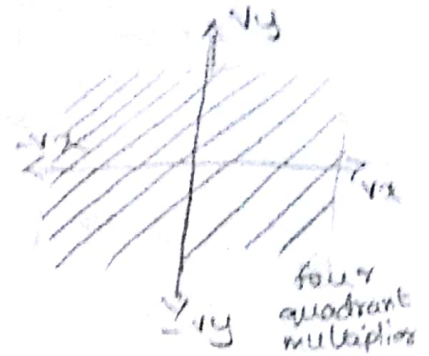
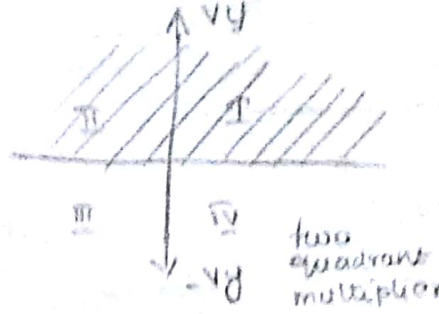
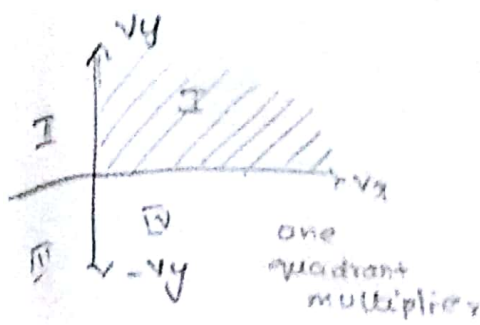
$$= 2 \sqrt{\frac{f_L K_V K_1 K_2 \pi}{2}}$$

$$\text{capture range} = \sqrt{2 \cdot f_L K_V K_1 K_2 \pi}$$



Analog Multiplier: (multiply 2 signal)

IC 533 } It considers the +ve & -ve i/p.
IC 534 }



Analog multiplier take 2 i/p and provides o/p as product of the i/p.

The Monolithic analog multiplier available IC 533 and IC 534. It uses transconductance technique. The symbol of IC is :

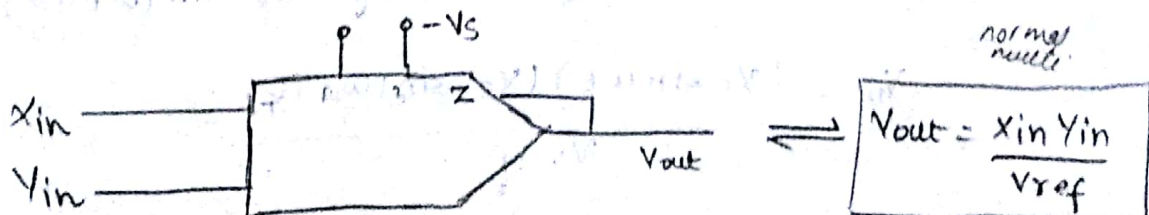
If both V_x and V_y +ve, then it is one quadrant multiplier. For 2 quadrant multiplier any one of the i/p must be +ve. For 4 quadrant multiplier i/p's can be either +ve or -ve.

IC 533:

Application

Z_{in}	1	14	$+V_s$
V_{out}	2	13	V_{pn}
$-V_s$	3	12	V_b
NC	4	11	Z_o
NC	5	10	End
NC	6	9	X_{out}
X_{in}	7	8	NC

- 1) Squaring
- 2) Square root
- 3) Divider
- 4) frequency Doubling



Symbol of IC 533

$$V_o = \frac{V_1 V_2}{2 V_{ref}} \left[\cos(\omega t - \omega t + 0) - \cos(\omega t + \omega t + 0) \right]$$

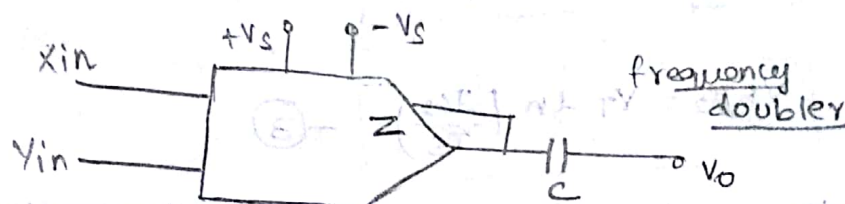
$$V_o = \frac{V_1 V_2}{2 V_{ref}} \left[\cos(0) - \cos(2\omega t + 0) \right]$$

If $\theta = 0$ $\cos(0) = 1$

$$V_o = \frac{V_1 V_2}{2 V_{ref}} - \frac{V_1 V_2}{2 V_{ref}} \cos(2\omega t)$$

↓
DC Component

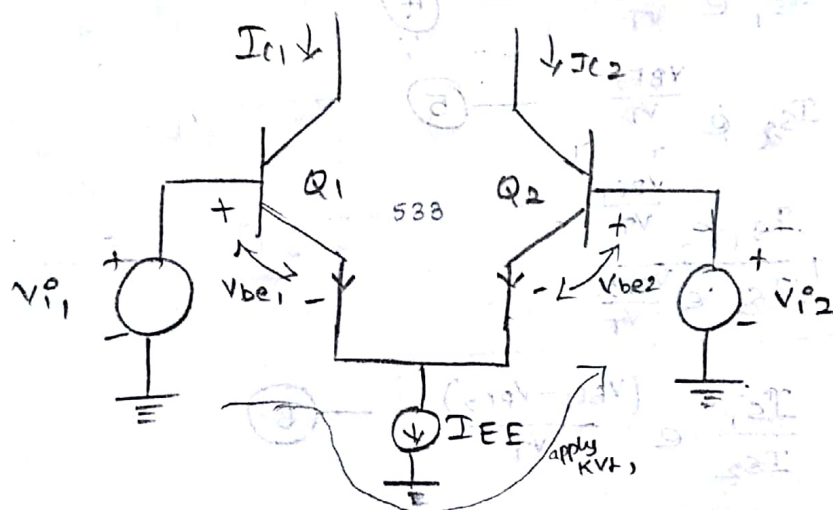
to remove this dc component add capacitor.



Analog multiplier using emitter coupled transistor pair:

kind of differential amplifier

535
analog multiplier



Q2/18

It has 2 transistors Q_1 & Q_2 whose emitters are tied together. And supplied by an constant current source, the o/p's are related by the differential i/p voltage,

Apply KVL, at

$$V_{i1} - V_{BE1} + V_{BE2} - V_{i2} = 0$$

$$V_{i1} - V_{i2} = V_{BE1} - V_{BE2} \quad \text{--- (1)}$$

Let, V_{BE1} be the applied voltage of the transistor

from the transistor,

$$I_{C1} = I_S e^{\frac{V_{BE1}}{V_T}} \quad (\eta=1)$$

I_S = saturation current or leakage current

taking $\ln$ on both sides,

$$\frac{I_{C1}}{I_S} = e^{\frac{V_{BE1}}{V_T}}$$

$$\rightarrow \ln \left(\frac{I_{C1}}{I_S} \right) = \frac{V_{BE1}}{V_T}$$

$$V_{BE1} = V_T \ln \left(\frac{I_{C1}}{I_S} \right) \quad - (2)$$

Similarly

$$V_{BE2} = V_T \ln \left(\frac{I_{C2}}{I_S} \right) \quad - (3)$$

Consider the transistors are not symmetrical and they possess different I_{S1} & I_{S2} .

By Diode current equation,

$$I_{C1} = I_{S1} e^{\frac{V_{BE1}}{V_T}} \quad - (4)$$

$$I_{C2} = I_{S2} e^{\frac{V_{BE2}}{V_T}} \quad - (5)$$

$\div$

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{S1} e^{\frac{V_{BE1}}{V_T}}}{I_{S2} e^{\frac{V_{BE2}}{V_T}}}$$

$$e^{a/b} = e^{a \cdot \frac{1}{b}}$$

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{S1}}{I_{S2}} e^{\frac{(V_{BE1} - V_{BE2})}{V_T}} \quad - (6)$$

$$V_{PD} = V_{BE1} - V_{BE2}$$

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{S1}}{I_{S2}} e^{\frac{V_{PD}}{V_T}} \quad - (7)$$

for common emitter amplification factor
 $\alpha = \frac{I_C}{I_E}$
 $\alpha = I_C / I_E$

The amplification factor $\alpha = \frac{O/P}{I/P} = \frac{I_C}{I_E}$

$$I_E = \frac{I_C}{\alpha}$$

$$-(I_{E1} + I_{E2}) = \frac{(I_{C1} + I_{C2})}{\alpha}$$

Assume $\alpha = 0.99 \approx 1$

Therefore,

$$I_{EE} = -(I_{E1} + I_{E2}) = (I_{C1} + I_{C2}) \quad \text{--- (8)}$$

If saturation current are made equal then, equ (7)

become, $I_{C1} = I_{C2} e^{v_{id}/V_T} \quad \text{--- (9)}$

from equ (8)

$$I_{EE} = I_{C1} + I_{C2}$$

$$I_{C2} = I_{EE} - I_{C1} \quad \text{--- (10)}$$

equ (9),

$$I_{C1} = (I_{EE} - I_{C1}) e^{v_{id}/V_T}$$

$$I_{C1} = I_{EE} e^{v_{id}/V_T} - I_{C1} e^{v_{id}/V_T}$$

$$I_{C1} + I_{C1} e^{v_{id}/V_T} = I_{EE} e^{v_{id}/V_T}$$

$$I_{C1} [1 + e^{v_{id}/V_T}] = I_{EE} e^{v_{id}/V_T}$$

$$I_{C1} = \frac{I_{EE} e^{v_{id}/V_T}}{1 + e^{v_{id}/V_T}}$$

$$I_{C1} = \frac{I_{EE}}{\frac{1 + e^{v_{id}/V_T}}{e^{v_{id}/V_T}}} = \frac{I_{EE}}{\frac{1}{e^{v_{id}/V_T}} + 1}$$

$$I_{C1} = \frac{I_{EE}}{1 + e^{-v_{id}/V_T}} \quad \text{o/p collector current --- (11)}$$

From equ (9) + (8)

$$I_{C1} = I_{EE} - I_{C2}$$

$$I_{C1} = I_{C2} e^{v_{id}/V_T}$$

$$(I_{EE} - I_{C2}) = I_{C1}$$

$$(I_{EE} - I_{C2}) = I_{C2} e^{v_{id}/V_T}$$

$$I_{EE} = I_{C2} e^{v_{id}/V_T} + I_{C2}$$

$$I_{EE} = I_{C2} [e^{v_{id}/V_T} + 1]$$

$$I_{C2} = \frac{I_{EE}}{[1 + e^{v_{id}/V_T}]} \quad \text{--- (12)}$$

Differential o/p current ΔI_C

$$\Delta I_C = I_{C1} - I_{C2}$$

sub (11) + (12)

$$\Delta I_C = \frac{I_{EE}}{1 + e^{-v_{id}/V_T}} - \frac{I_{EE}}{1 + e^{v_{id}/V_T}}$$

$$v_{id}/V_T = x$$

$$\Delta I_C = \frac{I_{EE}}{1 + e^{-x}} - \frac{I_{EE}}{1 + e^x}$$

$$\Delta I_C = \frac{I_{EE} [1 + e^x - 1 - e^{-x}]}{(1 + e^{-x})(1 + e^x)}$$

$$\Delta I_C = \frac{I_{EE} [e^x - e^{-x}]}{(1 + e^{-x})(1 + e^x)} \quad \text{--- (13)} = \frac{I_{EE} (e^x - e^{-x})}{(1 + e^{-x})(1 + e^x)}$$

consider only the denominator term

(a) $1 + e^x = e^{-x/2} \cdot e^{x/2} + e^{x/2} \cdot e^{x/2}$

(b) $1 + e^{-x} = e^{-x/2} \cdot e^{x/2} + e^{-x/2} \cdot e^{-x/2}$

multiply (a) & (b)

$$(e^{-x/2} e^{x/2} + e^{x/2} e^{x/2}) (e^{-x/2} e^{x/2} + e^{-x/2} e^{-x/2})$$

$$e^{x/2} (e^{-x/2} + e^{x/2}) e^{-x/2} (e^{x/2} + e^{-x/2})$$

$$\frac{e^{x/2} e^{-x/2}}{1} (e^{-x/2} + e^{x/2}) (e^{x/2} + e^{-x/2})$$

$$D.N = (e^{-x/2} + e^{x/2}) (e^{x/2} + e^{-x/2}) \quad \text{--- (14)}$$

Numerator: (NM)

$$e^x - e^{-x} = (e^{x/2} + e^{-x/2}) (e^{x/2} - e^{-x/2}) \quad \text{--- (15)}$$

sub (14) & (15) in (13)

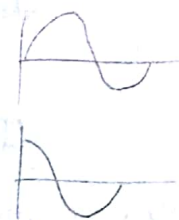
$$\Delta I_C = \frac{I_{EE} (e^{x/2} + e^{-x/2}) (e^{x/2} - e^{-x/2})}{(e^{-x/2} + e^{x/2})}$$

$$\Delta I_C = \frac{I_{EE} (e^{x/2} - e^{-x/2})}{(e^{-x/2} + e^{x/2})}$$

$\left[\frac{e^a - e^{-a}}{e^a + e^{-a}} = \frac{\sin}{\cos} = \tanh a \right]$
 op $\rightarrow \tan$
 no $\rightarrow \tanh$

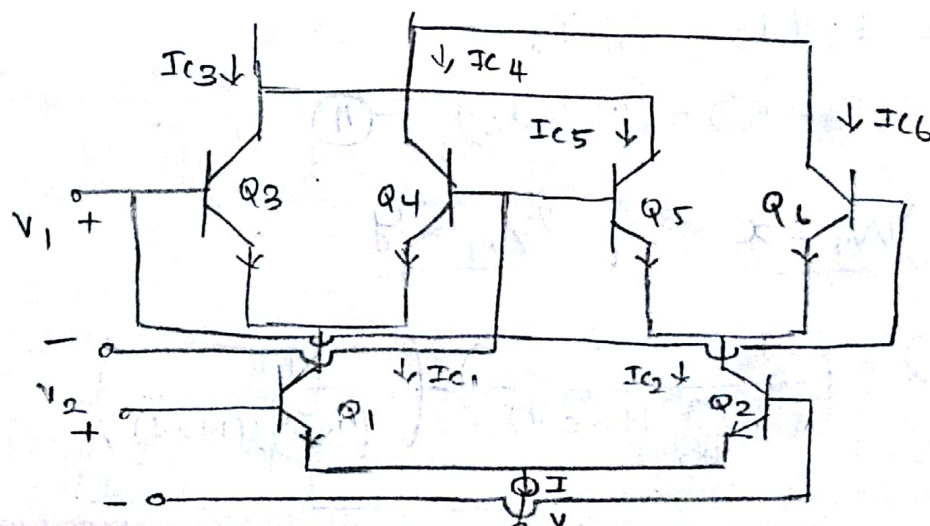
$$\Delta I_C = I_{EE} \tanh \frac{x}{2}$$

$$\Delta I_C = I_{EE} \tanh \left(\frac{V_{id}}{2V_T} \right)$$



$\downarrow$
 tan
 sec
 cosec
 cot
 } all the waveform

Q12/18 Gilbert Multiplier Cell:



This is the balanced multiplier. It consists of series connection of emitter coupled, 2 cross coupled transistor.

We have 6 transistor $Q_1, Q_2, \dots, Q_6$ and has corresponding currents $I_{C1}, \dots, I_{C6}$.

In previous derivation,

$$I_{C1} = \frac{I_{EE}}{1 + e^{-V_2/V_T}} \quad \text{--- (1)} \quad \text{Q1, Q2} \rightarrow \text{voltage } V_2 \text{ (from diagram)}$$

$$I_{C2} = \frac{I_{EE}}{1 + e^{V_2/V_T}} \quad \text{--- (2)}$$

by standard eqn, the collector current from Q_3, Q_4, Q_5, Q_6 are

$$I_{C3} = \frac{I_{C1}}{1 + e^{-V_1/V_T}} \quad \text{--- (3)} \quad I_{C5} = \frac{I_{C2}}{1 + e^{+V_1/V_T}} \quad \text{--- (5)}$$

$$I_{C4} = \frac{I_{C1}}{1 + e^{V_1/V_T}} \quad \text{--- (4)} \quad I_{C6} = \frac{I_{C2}}{1 + e^{-V_1/V_T}} \quad \text{--- (6)}$$

Now sub (1) in 3, 4 & (2) in 5, 6

$$I_{C3} = \frac{I_{EE}}{(1 + e^{-V_1/V_T})(1 + e^{-V_2/V_T})} \quad \text{--- (7)} \quad I_{C5} = \frac{I_{EE}}{(1 + e^{+V_1/V_T})(1 + e^{V_2/V_T})} \quad \text{--- (9)}$$

$$I_{C4} = \frac{I_{EE}}{(1 + e^{V_1/V_T})(1 + e^{-V_2/V_T})} \quad \text{--- (8)} \quad I_{C6} = \frac{I_{EE}}{(1 + e^{-V_1/V_T})(1 + e^{V_2/V_T})} \quad \text{--- (10)}$$

$$\Delta I = I_{(3-5)} \text{ to } I_{(4-6)}$$

$$= (I_3 + I_5) - (I_4 + I_6)$$

$$= I_3 + I_5 - I_4 - I_6$$

$$\Delta I = (I_3 - I_6) - (I_4 - I_5) \quad \text{--- (11)}$$

$$\underline{V_1/V_T = x}$$

$$\underline{V_2/V_T = y}$$

$$(I_3 - I_6) = \left(\frac{I_{EE}}{(1 + e^{-x})(1 + e^{-y})} \right) - \left(\frac{I_{EE}}{(1 + e^x)(1 + e^y)} \right)$$

$$= \frac{I_{EE}}{1+e^{-x}} \left[\frac{1}{(1+e^{-y})} - \frac{1}{(1+e^y)} \right]$$

$$I_3 - I_6 = \frac{I_{EE}}{1+e^{-x}} \left[\frac{e^y - e^{-y}}{(1+e^{-y})(1+e^y)} \right] \quad \text{--- (12)}$$

$$I_4 - I_5 = \left(\frac{I_{EE}}{(1+e^x)(1+e^{-y})} \right) - \left(\frac{I_{EE}}{(1+e^x)(1+e^y)} \right)$$

$$= \frac{I_{EE}}{(1+e^x)} \left[\frac{1}{(1+e^{-y})} - \frac{1}{(1+e^y)} \right]$$

$$I_4 - I_5 = \frac{I_{EE}}{(1+e^x)} \left[\frac{e^y - e^{-y}}{(1+e^{-y})(1+e^y)} \right] \quad \text{--- (13)}$$

sub (12) & (13) in (11)

$$\Delta I = (I_3 - I_6) - (I_4 - I_5)$$

$$= \left[\frac{I_{EE}}{1+e^{-x}} \left(\frac{e^y - e^{-y}}{(1+e^{-y})(1+e^y)} \right) \right] - \left[\frac{I_{EE}}{1+e^x} \left(\frac{e^y - e^{-y}}{(1+e^{-y})(1+e^y)} \right) \right]$$

$$= \frac{e^y - e^{-y}}{(1+e^{-y})(1+e^y)} \left[\frac{I_{EE}}{(1+e^{-x})} - \frac{I_{EE}}{(1+e^x)} \right]$$

$$= I_{EE} \left(\frac{e^y - e^{-y}}{(1+e^{-y})(1+e^y)} \right) \left(\frac{1}{(1+e^{-x})} - \frac{1}{(1+e^x)} \right)$$

$$\Delta I = I_{EE} \left[\frac{e^y - e^{-y}}{(1+e^{-y})(1+e^y)} \right] \left[\frac{e^x - e^{-x}}{(1+e^{-x})(1+e^x)} \right]$$

Refer eqn (13) in previous derivation,

$$\Delta I = I_{EE} \tanh x/2 \tanh y/2$$

$$\boxed{\Delta I = I_{EE} \tanh \frac{V_1}{2V_T} \tanh \frac{V_2}{2V_T}}$$

$$\left[\frac{e^x - e^{-x}}{(1+e^{-x})(1+e^x)} \right] = \tanh x/2$$

$$x = V_1/V_T$$

$$y = V_2/V_T$$

22/2/18 Applications of Gilbert Multiplier cell:

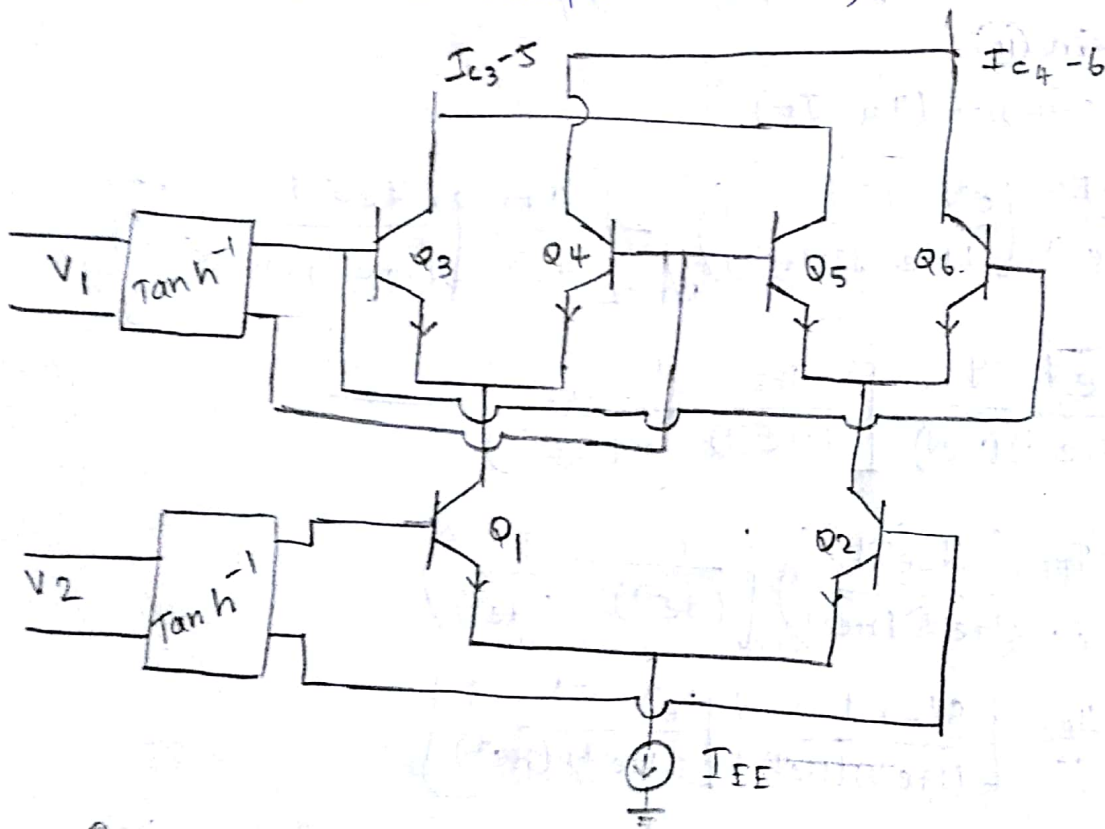
① When $V_1 > \tanh \frac{V_1}{2V_T}$ $\tanh \frac{V_1}{2V_T} \approx \frac{V_1}{2V_T}$
When $V_2 > \tanh \frac{V_2}{2V_T}$ $\tanh \frac{V_2}{2V_T} \approx \frac{V_2}{2V_T}$

$$\Delta I = I_{EE} \cdot \frac{V_1}{2V_T} \cdot \frac{V_2}{2V_T}$$

It can act as a perfect multiplier

- ② It act as a modulator for an input of square wave.
③ It can act as a phase detector

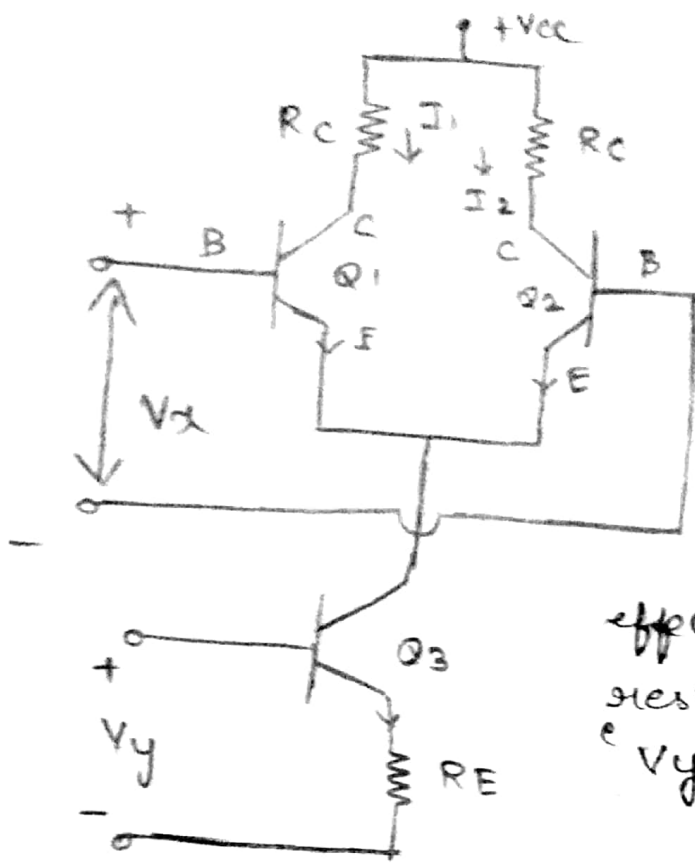
Complete Gilbert Multiplier cell is,



~~Variable~~ Transconductance Analog Multiplier.

This is the four quadrant multiplier.

i.e) the o/p is product of 2 i/p's irrespective of the polarity.



$$g_m = I/V$$

The transconductance effect ' g_m ' varies with respect to the 2nd input ' V_y '.

$$g_m = \frac{I_{EE}}{V_T} \quad \text{--- (1)}$$

$$I_{EE} = \frac{V_y}{R_E} \quad \text{--- (2)}$$

$$g_m = \frac{V_y}{R_E V_T} \quad \text{--- (3)}$$

If $V_x > V_y$

$$V_o = g_m R_C \cdot V_x \quad \text{--- (4)}$$

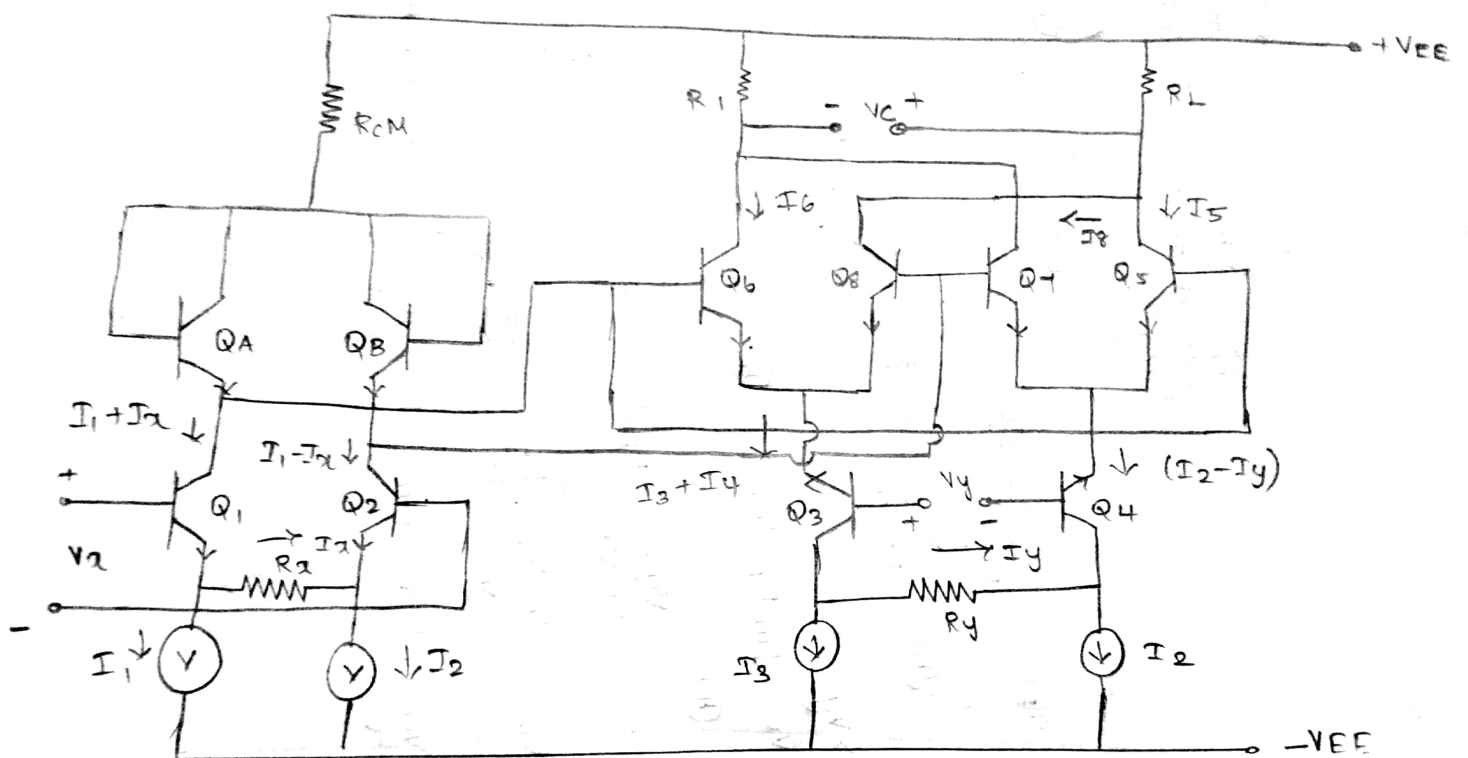
sub (3) in (4)

$$V_o = \frac{V_y}{R_E V_T} \cdot R_C \cdot V_x$$

$$V_o = \frac{V_x V_y}{V_T} \frac{R_C}{R_E} \quad \text{--- (5)}$$

If $V_x < V_y$, there won't be any emitter current.

Complete Gilbert Multiplier:



The 1st part of the circuit generate a intermediate voltage V_1 across Q_A and Q_B . In response with the input V_x . The non-linear response in generating V_1 is compensated by Quad transistor. Quad transistor Q_5, Q_6, Q_7 and Q_8 . The o/p is maintained in linear with 2 inputs V_x, V_y . The Resistor R_x, R_y provides a linear conversion b/w i/p voltage V_x, V_y to the differential current the $\frac{V_x}{R_x} - I_x, I_y$ be, $\frac{V_x}{R_x} = I_x, I_y = \frac{V_y}{R_y}$

R_x, R_y should be chosen such that

$$R_x \gg \frac{V_x}{I_1} \quad R_y \gg \frac{V_y}{I_2}$$