DESIGN AND IMPLEMENTATION OF AN PID CONTROLLED EFFICIENT BUCK-BOOST CONVERTER USING INTERLEAVED TOPOLOGY

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***Abstract*—A DC-DC converter is of great importance in the field of sustainable energy. This paper deals with the Buck-Boost converter which converts a DC voltage to a higher value (step up) and also to a lower value (step down). But due to various switching losses, conduction losses across the passive elements, there is a reduction in efficiency which deteriorates the converter performance. Thus to avoid a Interleaved topology is employed. Where two buck-boost converters operate in parallel and reduce the switching stress and reduce the ripple content of the input current as the switches operate 180^o out of phase. Thus this paper analyses the efficiency and the output values of both Buck-Boost and Interleaved Buck-Boost converter and the results are simulated with the help of MATLAB / SIMULINK environment.**

Keywords: Buck-Boost converter; Interleaved Buck-Boost converter; Efficiency; Ripple cancellation.

1. INTRODUCTION

A suitable DC-DC converter is required for designing high efficiency power systems. Among the various topologies, Interleaved buck-boost converter is considered as a better solution for high power systems due to improved electrical performance, reduced weight and size. Detailed analysis has been done to investigate the benefits of interleaved buck-boost converter compared to the conventional buck-boost converter topologies.

Due to the current handling limitation of single switch, the output power is small, typically tens of watts. At a higher current, the size of these components increases, with increased component losses, and the efficiency decreases. The simplest way of describing a interleaved converter is to see it as consisting of several power stages (converter "phases") with inputs parallel and drive signals shifted to ensure uniform distribution over a switching period .

In pratical case there will be formation of harmonics and current ripples and voltage losses along the passive elements of the power converter. Hence the pratical values will be lesser than the calculated one.These losses can be reduced by using interleaved topology. Where the gate pulses to the transistors in parallel with the inductors are 180^o out of phase with each other with the same frequency thus the ripples in the input inductor current will get reduced. And thus the efficiency of the converter is improved than the conventional buck-boost converters.

2. BUCK-BOOST CONVERTER

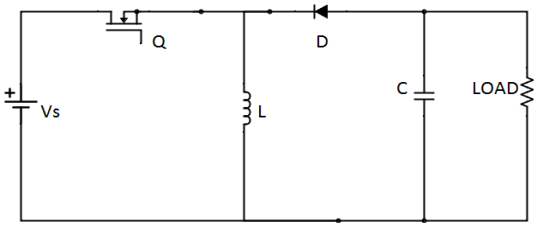

Fig. 1 Schematic diagram of Buck-Boost Converter

Buck-Boost converter belongs to the family of basic power conversion topologies (the other two being buck and buck-boost derivative). The schematic diagram of buck-boost converter is shown in Fig. 1. Buck-Boost converters are probably the most versatile paths to sustainable energy power converters today. It is typically used when output voltage can be made either higher or lower than the input voltage. It uses only one switch, employing only one stage conversion, and requires inductors and capacitors for energy transfer. It provides output voltage of reverse polarity. Hence care must be taken by switching the terminals while using the converted power for practical applications.

The relationship between the input voltage and the output voltage is

$$V_o = \frac{-V_s d}{1-d} \quad (1)$$

Where $d = \frac{T_{on}}{T}$ is the duty cycle ratio. T_{on} is the ON time of the semiconductor switch and T is the switching period. In continuous current mode of conduction the selected value of inductance should be greater than the critical value of the inductance L_c. The value of inductance L and capacitance C can be found by [1]:

$$\Delta I = \frac{V_s d}{fL} \quad (2)$$

$$\Delta V_c = \frac{I_o d}{fC} \quad (3)$$

Where ΔI is the ripple current, ΔV_c is the ripple voltage, f is the switching frequency, L is the filter inductance and C is the filter capacitance of the circuit.

3. INTERLEAVED BUCK-BOOST CONVERTER

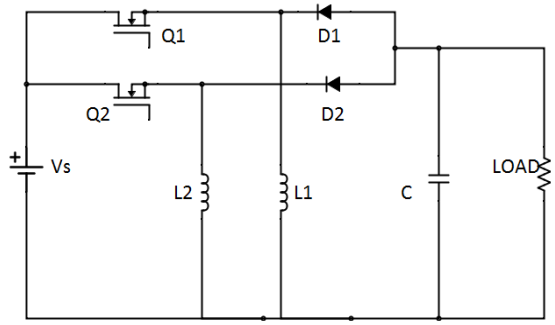

Fig. 2 Schematic diagram of Interleaved Buck-Boost Converter

Due to the current handling limitation of single switch, the output power is small, typically tens of watts. At a higher current, the size of these components increases, with increased component losses, and the efficiency decreases. The simplest way of describing a Interleaved converter is to see it as consisting of several power stages (converter "phases") with inputs and outputs connected in parallel and drive signals shifted to ensure uniform distribution over a switching period .

4. DESIGN CONSIDERATIONS

For designing the interleaved buck-boost power converter we must choose the appriopriate value for the inductor and capacitive filter used whose value is given by,

$$L1 = L2 = \frac{Vsd}{f\Delta I} \quad (4)$$

$$C = \frac{Iad}{f\Delta Vc} \quad (5)$$

Table 1. Design parameters of Interleaved Buck-Boost Converter

Parameter	Values
Input voltage(V_s)	10 V
Output voltage(V_o)	15 V
Output power(P_o)	25 W
Ripple voltage (ΔV_c)	0.017
Ripple current(ΔI_l)	4.645
Inductor (L1= L2)	52µH
Output capacitance	2.5 mF
Resistance(R_o)	9 Ω
Duty ratio (d)	60 %

In pratical case there will be formation of harmonics and current ripples and voltage losses along the passive elements of the power converter. Hence the pratical values will be lesser than the calculated one. These losses can be reduced by using interleaved topology.The inductor and capacitor values of the interleaved buck-boost converter is derived from equation (2) and (3).

4. SIMULATION RESULTS AND DISCUSSION

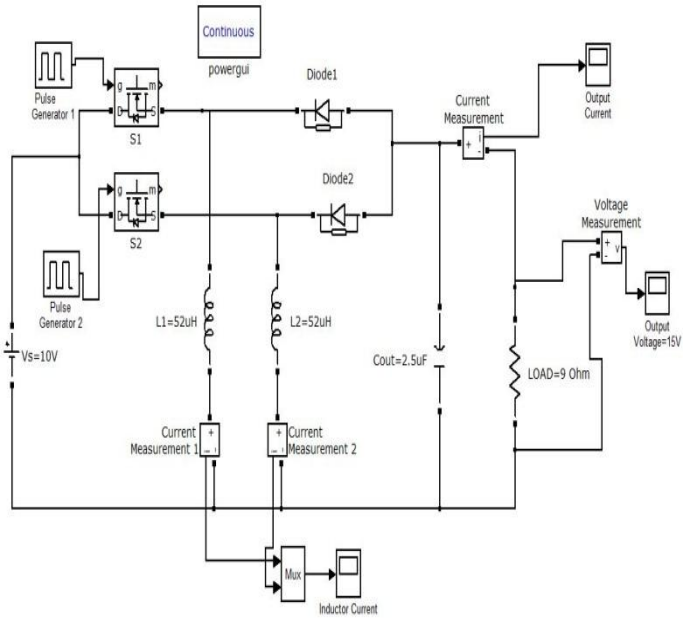

Fig. 3. MatLAB / Simulink diagram of Buck-Boost converter

The proposed interleaved buck-boost converter is simulated using MATLAB / SIMULINK is shown in Fig. 3. The ultimate aim is to achieve a ripple free high efficiency buck-boost converter operation. Where the gate pulses to the transistors in parallel are 180º out of phase with each other with the same frequency thus the ripples in the input inductor current will get reduced. The interleaved buck-boost converter is designed using Table II. The designed DC-DC converter simulated using Matlab is depicted in Fig. 3. Input inductor current L1 and L2 are given in Fig. 4. The MOSFETs are operated by 180º out of phase, the ripple present in the current are eliminated. The current from the inductors are out of phase with each other, hence 3rd order harmonics present in the current is eliminated. Hence the small value of capacitor is enough to eliminate the rest of the harmonics present in the load current.

The output voltage response of the buck-boost converter and interleaved buck-boost converter are given in Fig. 5. Both the circuits are simulated with the input voltage of 10 V and the duty cycle of the pulse given to the switches is 60 %. The obtained output voltage of the buck-boost converter is only 13.6 V, but the output voltage of the interleaved buck-boost converter is 15.05 V. Similarly the Output Current for the Buck-Boost converter is only 1.51A but it is 1.66 A in the case of an

Interleaved Buck Boost converter, which shows that there is an improved efficiency.

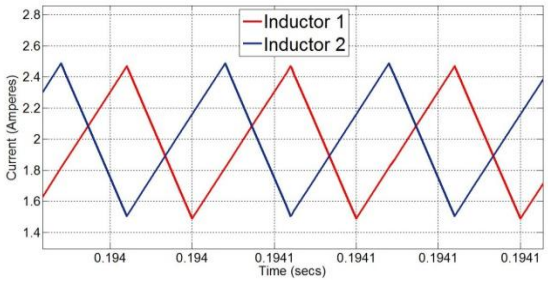

Fig. 4 Input Inductive current ripple cancellation

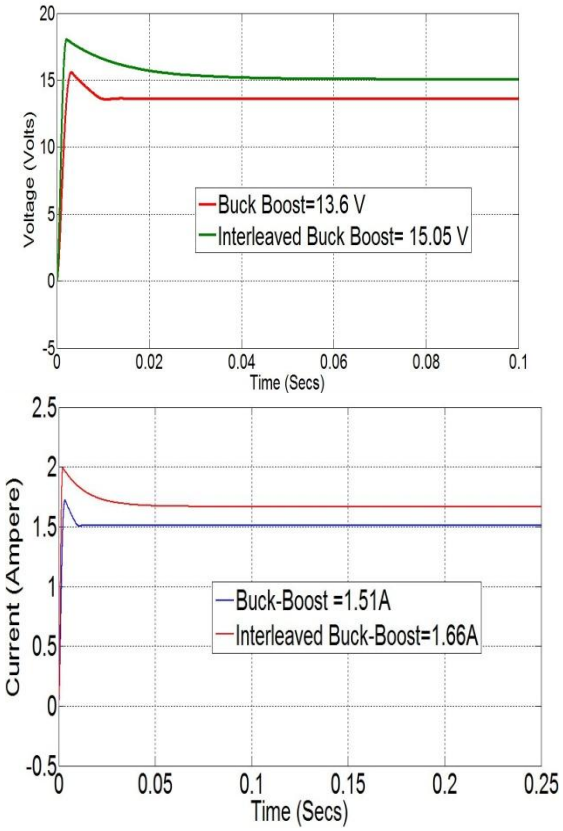

Fig. 5. Output Voltage and Output current of the Buck-Boost and Interleaved Buck-Boost Converter

Both the converter output consists of peak overshoot. This ripple cancellation helps to reduce the voltage drop and increase the output voltages in the conventional and interleaved Buck-Boost converter.

5. EFFICIENCY ANALYSIS

The efficiency calculation of the Buck-Boost and the interleaved Buck-Boost converter are given below: The equations corresponding to the calculations are,

$$\text{Efficiency} = \frac{\text{Pout}}{(\text{Pout}+\text{Ps}+\text{Pl}+\text{Pd})} \quad (6)$$

The conduction loss (P_{SC}) and switching loss (P_{ss}) of the MOSFET are

$$P_{SC} = Rs \times d \times (Ia/1 - d)^2 \quad (7)$$

$$P_{ss} = \frac{1}{2} f s V_s I_L (t_{on} + t_{off}) \quad (8)$$

$$PS = P_{SC} + P_{sd} \quad (9)$$

Where, Rs is MOSFET ON resistance, t_{on} is the ON time of the switch, t_{off} is the OFF time of the switch, d is the duty ratio, and I_L is the current through an inductor.

The conduction loss in the inductor (Pl)

$$Pl = RL \times (Ia/1 - \delta)^2 \quad (10)$$

The conduction loss (Pd) and switching loss (P_{sd}) of the diode

$$Pcd = R_D \times Ia^2 + VF \times Ia \quad (11)$$

$$P_{sd} = \frac{1}{2} f s V_s I_L (t_{on} + t_{off}) \quad (12)$$

$$Pd = Pcd + P_{sd} \quad (13)$$

Where, VF is the forward ON Voltage, R_D is the Diode resistance, and Ia is the output current.
Thus the input power

$$P_{IN} = Pout + Ps + Pl + Pd \quad (14)$$

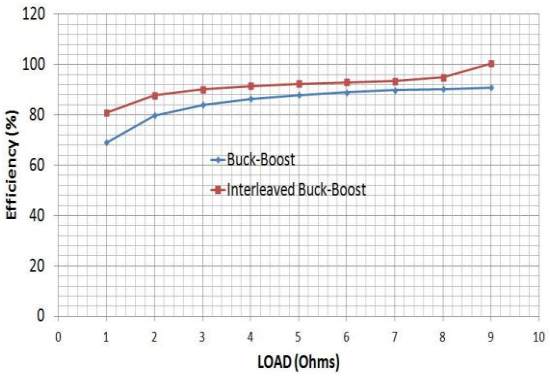

Fig. 6 Efficiency graph for buck-boost and interleaved buck-boost converter

Efficiency graph for buck-boost and interleaved buck-boost converter is portrayed in Fig. 10. The efficiency of both the converters are calculated using the equation (14) to (22). The load resistance is varied from 1 Ohm to 9 Ohm; the corresponding efficiency values are plotted. For every load resistance value efficiency of the interleaved buck-boost converter is higher than the conventional buck-boost converter. Thus it is evident from the above graph that the interleaving technique improves the efficiency of the Buck-Boost converter by 2% to 6%. As it reduces the ripple and reduces the heat dissipation of the inductor used.

.6. DESIGNING OF CLOSED LOOP PID CONTROLLER FOR INTERLEAVED BUCK-BOOST CONVERTER

For designing the closed loop PID controller for the converter state space modelling is done to determine the transfer function of the system and then by using Ziger Nicholas chart and Routh stability criterion the values proportional, Integral and Differential gains are determined and the stability of the controller is determined through MATLAB programs from which the closed loop is simulated by SIMULINK.

5.1 .State Space Modelling

There are four modes of operation for an interleaved buck-boost converter based on the ON/OFF state of the switches. Since this design deals only with two switches there are four states of operation which are tabulated below

Table 2. Modes Of Operation Of Interleaved Buck-Boost Converter

Mode	Q1	Q2
1	ON	ON
2	OFF	ON
3	ON	OFF
4	OFF	OFF

5.1.1 .Mode 1: Q1 and Q2 ON

In mode 1 operation, both transistors Q1 and Q2 are ON and diodes D1 and D2 are reverse biased. The inductor stores the supplied energy (1/2 LI^2).

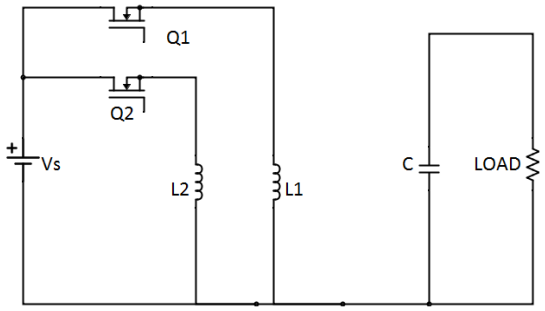

Fig. 7 Mode 1 Interleaved Buck-Boost Converter

The governing equations of mode 1 is expressed as

$$\frac{di_{L1}}{dt} = \frac{V_S}{L1} \quad (15)$$

$$\frac{di_{L2}}{dt} = \frac{V_S}{L2} \quad (16)$$

$$\frac{dV_o}{dt} = \frac{V_o}{RC} \quad (17)$$

The state space parameters for mode 1 are given by,

$$A1 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{RC} \end{bmatrix} \quad (18)$$

$$B1 = \begin{bmatrix} \frac{1}{L1} \\ \frac{1}{L2} \\ 0 \end{bmatrix} \quad (19)$$

5.1.2.Mode 2: Q1 OFF, and Q2 ON

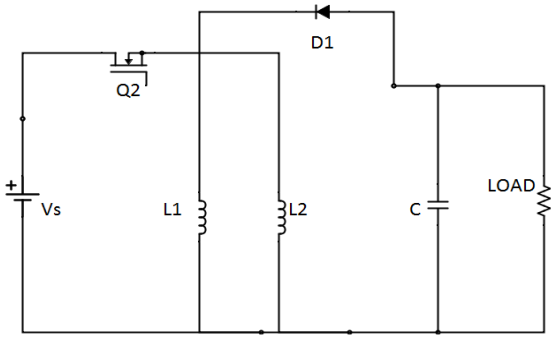

Fig. 8 Mode 2 Interleaved Buck-Boost Converter

In mode 2 the transistor Q1 is OFF and Q2 is ON and the diode D1 is forward biased and D2 is reversed biased. Thus L1 discharges to the capacitor C1.The governing equations of mode 2 can be described by:

$$\frac{di_{L1}}{dt} = \frac{V_o}{L1} \quad (19)$$

$$\frac{di_{L2}}{dt} = \frac{V_S}{L2} \quad (20)$$

$$\frac{dV_o}{dt} = \frac{i_{L1}}{C} - \frac{V_o}{RC} \quad (21)$$

The state space parameters for mode 2 are given by,

$$A2 = \begin{bmatrix} 0 & 0 & \frac{1}{L1} \\ 0 & 0 & 0 \\ \frac{-1}{C} & 0 & \frac{-1}{RC} \end{bmatrix} \quad (22)$$

$$B2 = \begin{bmatrix} \frac{1}{L1} \\ 0 \\ 0 \end{bmatrix} \quad (23)$$

5.1.3 Mode 3: Q1 ON, and Q2 OFF

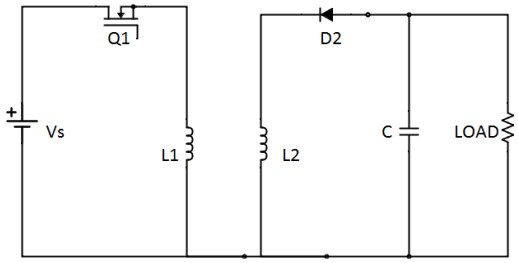

Fig. 9 Mode 3 Interleaved Buck-Boost Converter

In the mode 3 operation, the transistors Q1 ON and Q2 OFF and diode D1 reverse biased and D2 forward biased. Thus L2 discharges to the capacitor C1 The equivalent circuit equations are derived as

$$\frac{di_{L1}}{dt} = \frac{V_s}{L1} \quad (24)$$

$$\frac{di_{L2}}{dt} = \frac{V_s}{L2} \quad (25)$$

$$\frac{dV_o}{dt} = \frac{i_{L2}}{C} - \frac{V_o}{RC} \quad (26)$$

The state space parameters for mode 3 are given by,

$$A3 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L2} \\ 0 & \frac{-1}{C} & \frac{-1}{RC} \end{bmatrix} \quad (27)$$

$$B3 = \begin{bmatrix} 0 \\ \frac{1}{L2} \\ 0 \end{bmatrix} \quad (28)$$

5.1.4.MODE 4: Q1 OFF and Q2 OFF

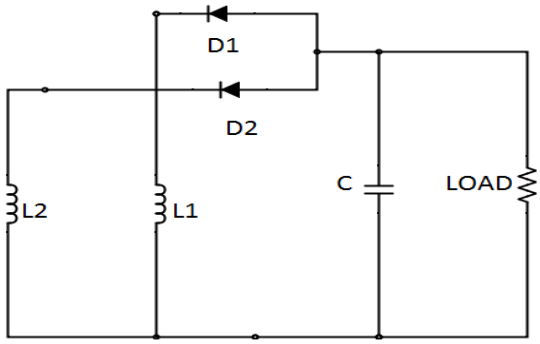

Fig. 10 Mode 4 Interleaved Buck-Boost Converter

Finally, during the Mode 4 operation, the transistors Q1 and Q2are OFF and the diodes D1 and D2 are forward biased Thus both the inductors L1 and L2 discharges to the capacitor C1. The equations of mode 4 are

$$\frac{di_{L1}}{dt} = \frac{V_o}{L1} \quad (29)$$

$$\frac{di_{L2}}{dt} = \frac{V_o}{L2} \quad (30)$$

$$\frac{dV_o}{dt} = \frac{i_{L1}}{C} + \frac{i_{L2}}{C} - \frac{V_o}{RC} \quad (31)$$

The state space parameters for mode 4 are given by,

$$A4 = \begin{bmatrix} 0 & 0 & \frac{1}{L1} \\ 0 & 0 & \frac{1}{L2} \\ \frac{-1}{C} & \frac{-1}{C} & \frac{-1}{RC} \end{bmatrix} \quad (32)$$

$$B4 = \begin{bmatrix} \frac{d1+d2}{L1} \\ \frac{d1+d3}{L2} \\ 0 \end{bmatrix} \quad (33)$$

Thus the state space equation for the entire system is given by,

A=A1*d1+ A2*d2+ A3*d3+ A4*d4 (34)

Therefore,

$$A = \begin{bmatrix} 0 & 0 & \frac{d3+d4}{L1} \\ 0 & 0 & \frac{d2+d4}{L2} \\ \frac{-(d3+d4)}{C} & \frac{-(d2+d4)}{C} & \frac{-1}{RC} \end{bmatrix} \quad (35)$$

Similarly,

B = B1*d1+ B2*d2+ B3*d3+ B4*d4 (35)

$$B = \begin{bmatrix} \frac{d1+d2}{L1} \\ \frac{d1+d3}{L2} \\ 0 \end{bmatrix} \quad (36)$$

And, As the controller is based on output voltage sensing,

C=[0 0 1] ; D=[0]

Thus the state space model is given by,

X'=AX+BU ; and Y=CX'+DU. Where,

$$X = \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_o \end{bmatrix} \quad (37)$$

$$X' = \frac{dX}{dt} = \begin{bmatrix} i'_{L1} \\ i'_{L2} \\ V'_o \end{bmatrix} \quad (38)$$

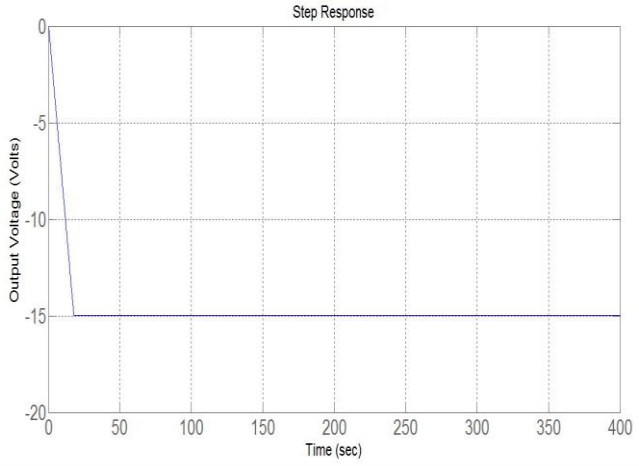

Fig 11. step response of the transfer function

Thus from the derived state space model we can get the transfer function and its response given by,

6.679e-013 s^2 - 3.692e006 s + 7.824e-008
---------- (39)
s^3 + 44.44 s^2 + 2.462e006 s + 2.708e-008

The step response of the transfer function is given below. The Characteristics equation is given by,

1+G(s).H(s) = 0 (40)

Now, by using Routh stability criterion and Ziger Nicolas chart the values of proportional, Integral and Differential gains are determined which are given by,

K_p=1 ; K_i=7e10 ; K_d=1e6

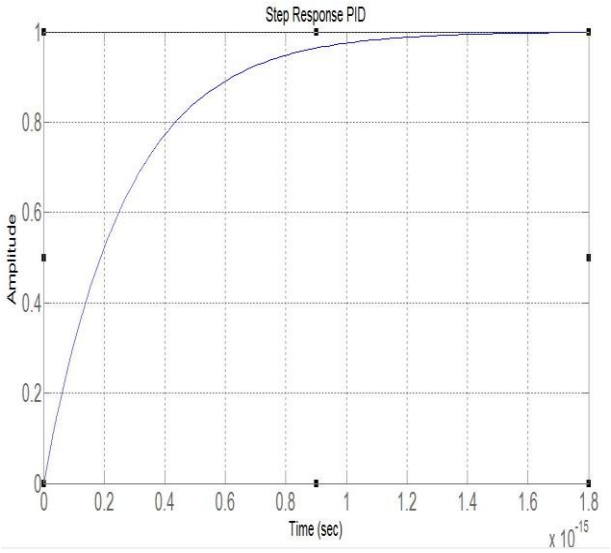

Fig 12. Step response of PID controller

Thus from the above response the system seems to be stable at an settling time of 1.6 feta secs.

7. SIMULATION AND RESULTS OF CLOSED LOOP PID CONTROLLED INTERLEAVED BUCK-BOOST CONVERTER

The calculated values are simulated using SIMULINK and the result are shown,

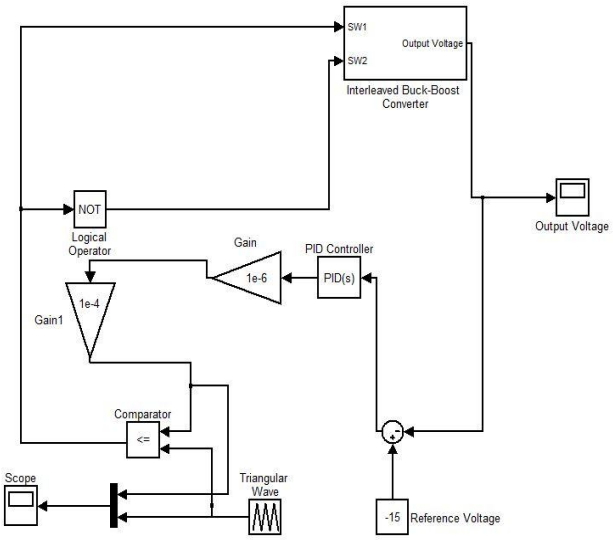

Fig 13. SIMULINK diagram of PID Controller

The above figure shows the SIMULINK diagram of PID closed loop simulation the results of the simulations are shown below.

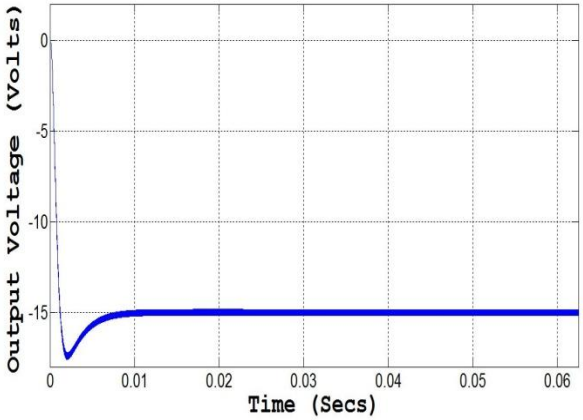

Fig 14. Output Boost Configuration

The above figure shows the output when the reference is 15V which is the boost configuration.

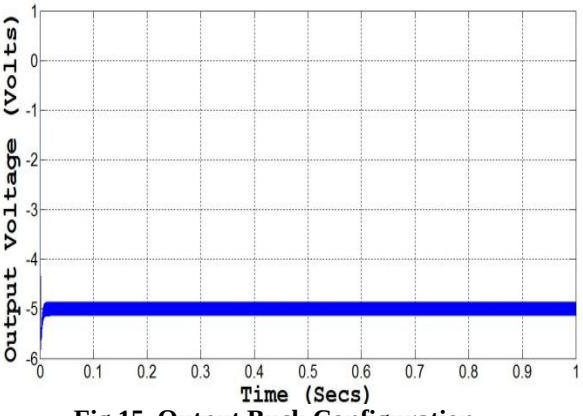

Fig 15. Output Buck Configuration

The above figure shows the output when the reference is 5V which is the buck configuration.

7. .HARDWARE IMPLEMENTATION

This project deals with the Open loop Configuration of Interleaved Buck-Boost Converter alone for hardware implementation. For the hardware the converter prototype is designed for 1Watt.The corresponding PCB (Printed Circuit Board) are fabricated which involves the following components

1. Mosfet-2 Pieces-IRF840
2. Inductor 1.5H -2 Pieces
3. Capacitor 10µF -1 Piece
4. Mosfet Driver IC- TLP250- 2 Pieces
5.

The Mosfet Driver is used to amplify the gate pulse voltage to the Mosfet threshold needs by push pull amplification.
The schematic of TLP250is shown below,

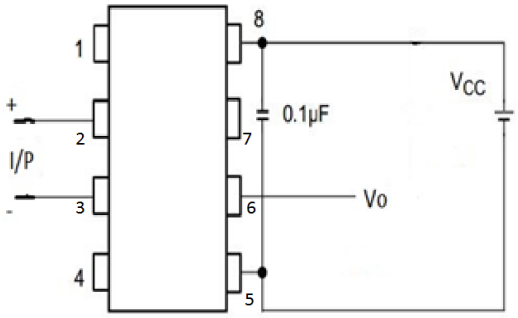

Fig 16. Schematic of TLP250 Mosfet driver

It should be noted that the Vcc bust be between 12V to 20V which is the operating range of the driver. A capacitor is connected across the supply pins to filter the ripples in the supply. Pins 2 and 3 forms the input and Pin 6 is the output pin which is connected to the gate of the mosfet. The hardware is implemented and the results are shown below.

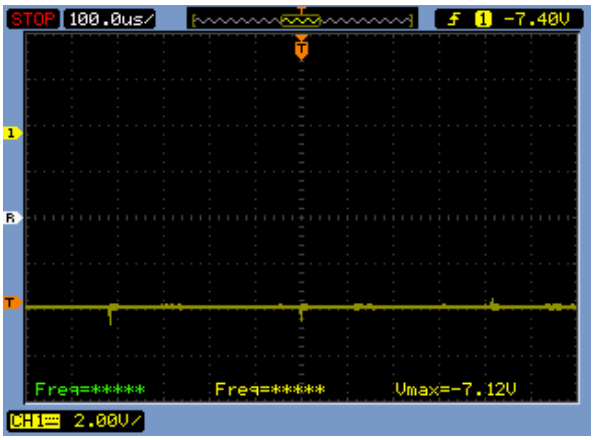

Fig 17. Boost operation 60% duty cycle

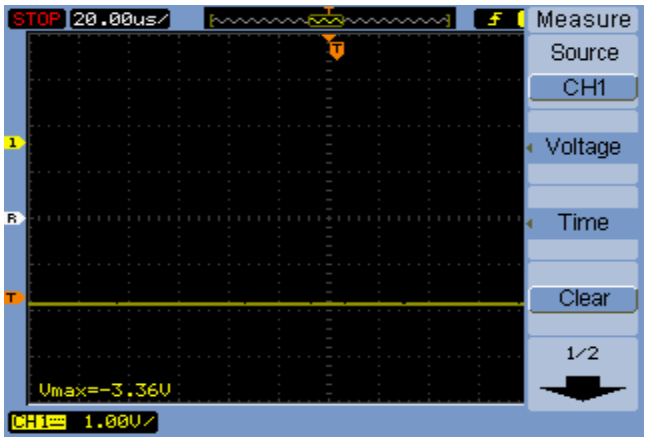

Fig 18. Buck operation 40% duty cycle

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